

Model Name: GA-B85M-D3H

SHEET TITLE Revision 1.12

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1150-A
05	CPU_LGA1150-B
06	CPU_LGA1150-C
07	DDR III CHANNEL A 1,2
08	DDR III CHANNEL B 1,2
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESS*4 SLOT
16	PCI SLOT1,2
17	ITE 8728 LPC IO
18	COM,KB_MS_USB,USB30_20
19	HWM,FAN CTRL,OV,-PROCHOT
20	DUAL BIOS
21	FP,FUSB,SPK,SATALED
22	Realtek ALC892-GR
23	REAR AUDIO JACK
24	REALTEK RTL8111F
25	DISCRETE POWER
26	ATX , CLOCK GEN, TPM
27	VCORE ISL95820_1

SHEET TITLE

28	VCORE ISL95820_2
29	RT8120_DDR POWER
30	LPT, M3 POWER
31	DVI, HDMI
32	IT8892E

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Gigabyte Technology		
Title		
Cover Sheet		
Size	Document Number	Rev
Custom	GA-B85M-D3H	1.12
Date:	Wednesday, June 18, 2014	Sheet 1 of 32

Model Name: GA-B85M-D3H

Component value change history

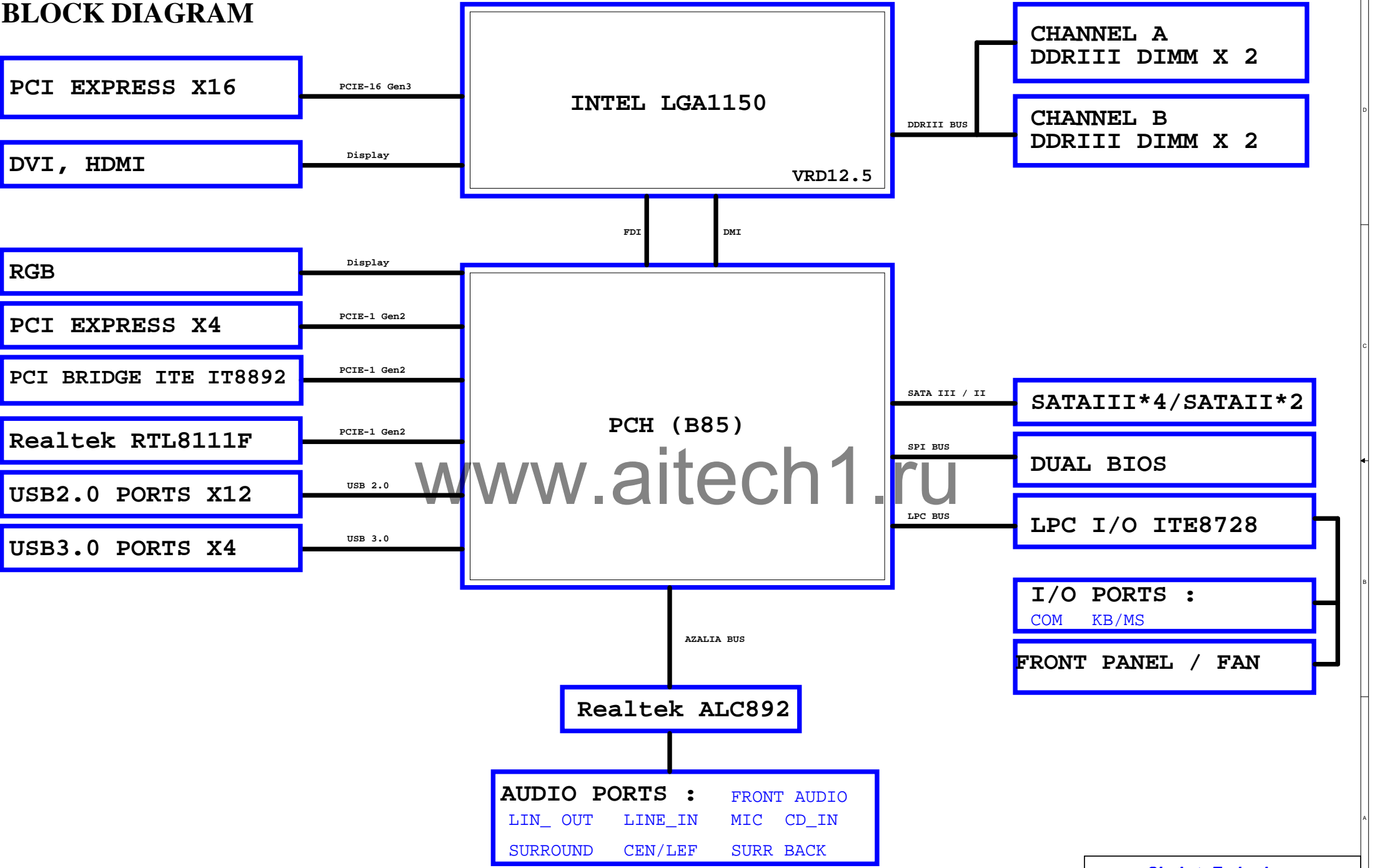
Revision 1.12
P-Code U12090-0

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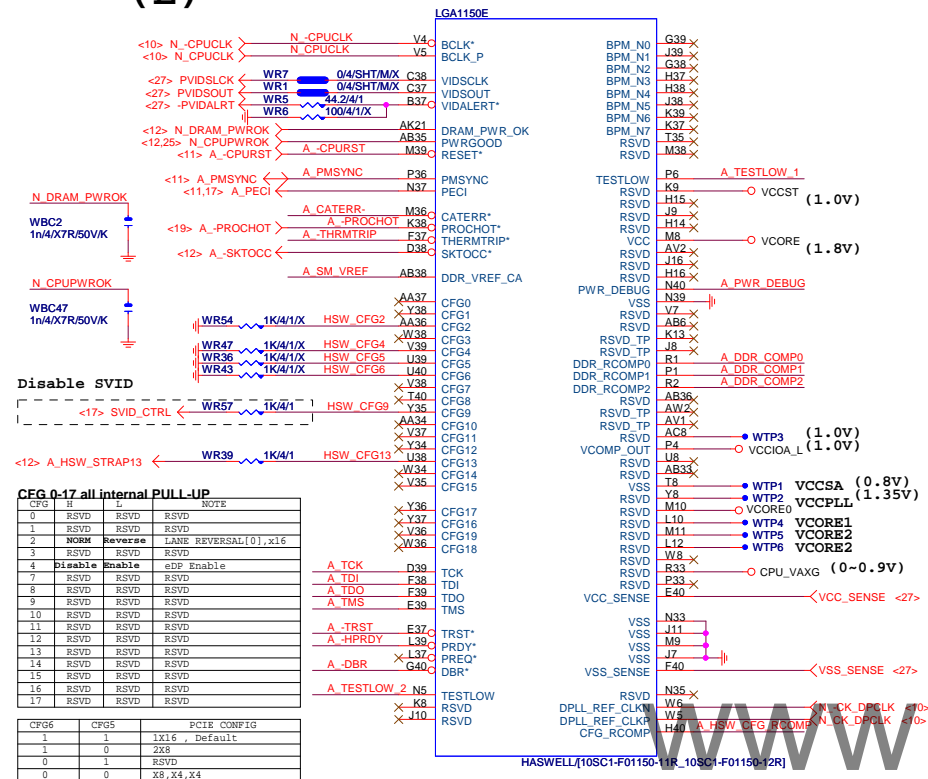
Circuit or PCB layout change

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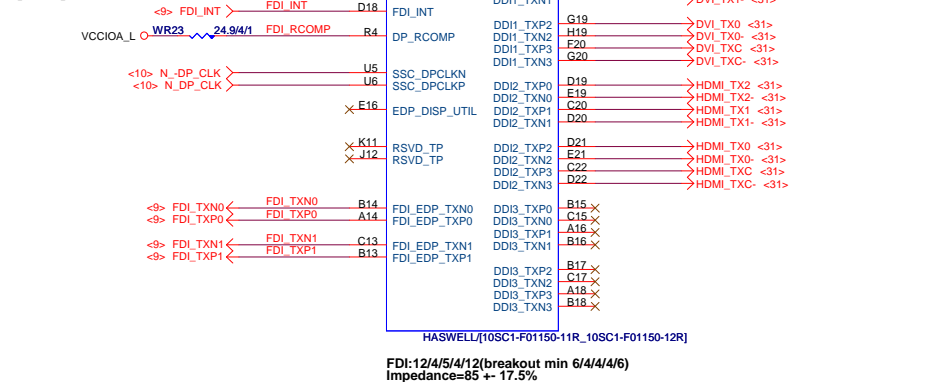
BLOCK DIAGRAM



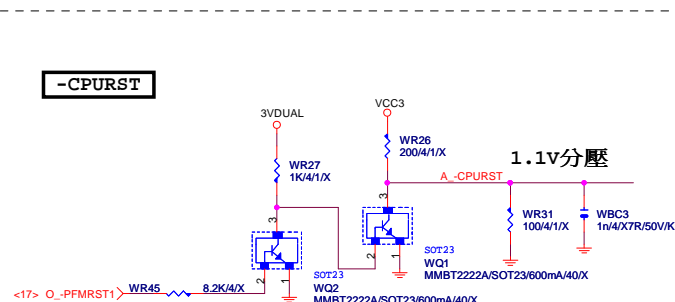
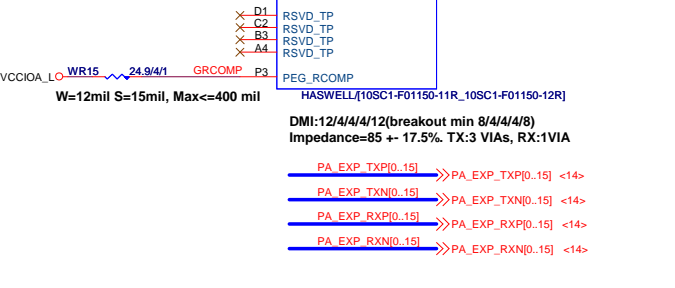
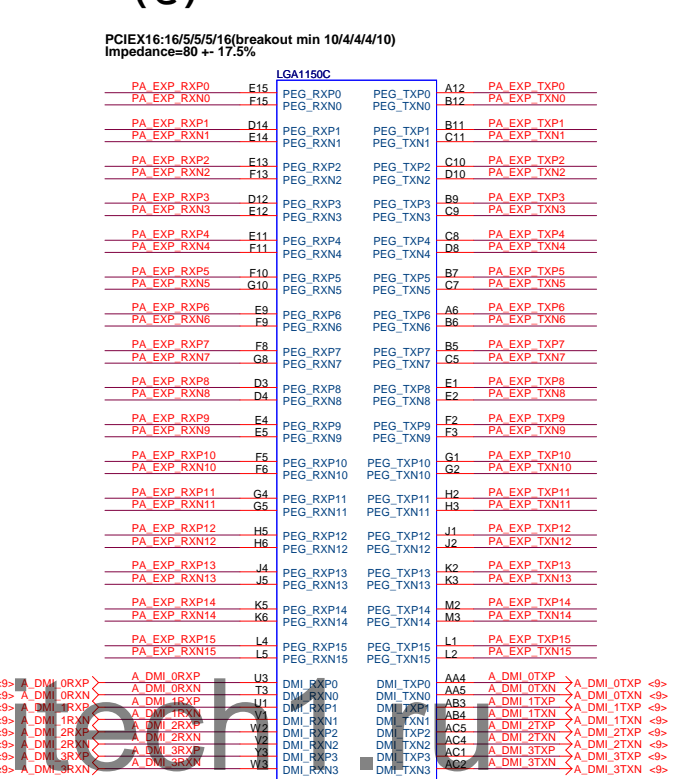
LGA1150 (E)



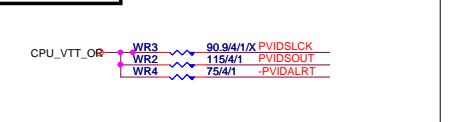
LGA1150 (D)



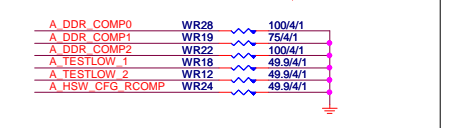
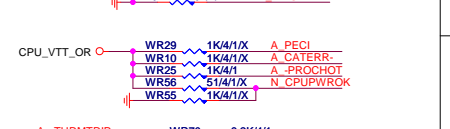
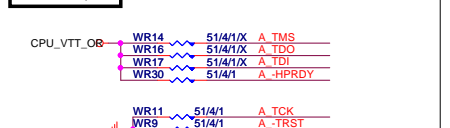
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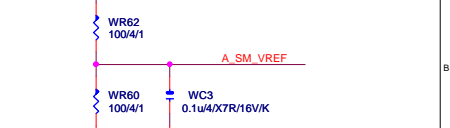
CPU SVID



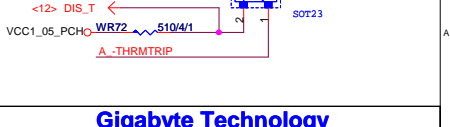
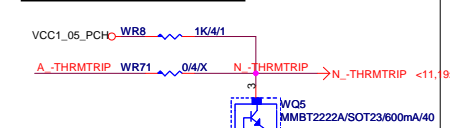
CPU PU/PD



SM REF



THRMTRIP DISABLE



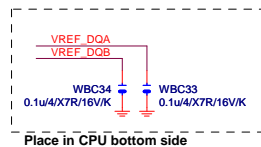
LGA1150 (A)

LGA1150A									
	MAAA0	AU13		DDRO_D0	AD38	MDA0			
	MAAA1	AV16		DDRO_D1	AD39	MDA1			
	MAAA2	AW18		DDRO_D2	AF38				
	MAAA3	AW17		DDRO_D3	AF39	MDA3			
	MAAA4	AU17		DDRO_D4	AD37	MDA4			
	MAAA5	AW18		DDRO_D5	AD40	MDA5			
	MAAA6	AV17		DDRO_D6	AF37	MDA6			
	MAAA7	AT18		DDRO_D7	AF40	MDA7			
	MAAA8	AU18		DDRO_D8	AD39	MDA9			
	MAAA9	AT19		DDRO_D9	AD38	MDA10			
	MAAA10	AW11		DDRO_D10	AK39	MDA11			
	MAAA11	AU19		DDRO_D11	AK38				
	MAAA12	AU19		DDRO_D12	AK37	MDA12			
	MAAA13	AV10		DDRO_D13	AK39				
	MAAA14	AT20		DDRO_D14	AK40	MDA14			
	MAAA15	AU21		DDRO_D15	AK40	MDA15			
				DDRO_D16					
	MODT_A0	AW10		DDRO_D17	AM39	MDA21			
	MODT_A1	AY8		DDRO_D18	AP38	MDA18			
	MODT_A2	AU9		DDRO_D19	AP39	MDA19			
	MODT_A3	AW8		DDRO_D20	AM39	MDA20			
				DDRO_D21	AK38	MDA16			
				DDRO_D22	AP37	MDA22			
		AW33		DDRO_D23	AP40	MDA23			
		AU33		DDRO_D24	AV37	MDA25			
		AU31		DDRO_D25	AW37	MDA29			
		AV31		DDRO_D26	AK35	MDA26			
		AT33		DDRO_D27	AV35	MDA27			
		AU33		DDRO_D28	AM37	MDA28			
		AT31		DDRO_D29	AT37	MDA24			
		AW31		DDRO_D30	AD35	MDA30			
				DDRO_D31	AW35	MDA31			
				DDRO_D32	AY6	MDA33			
<->	SBA0	AV12		DDRO_D33	AY6	MDA37			
<->	SBA1	AT11		DDRO_D34	AV4	MDA34			
<->	SBA2	AY1		DDRO_D35	AD4	MDA35			
				DDRO_D36	AW6	MDA36			
<->	CKEA0	AV22		DDRO_D37	AW3	MDA32			
<->	CKEA1	AT23		DDRO_D38	AW4	MDA38			
<->	CKEA2	AU22		DDRO_D39	AY4	MDA39			
<->	CKEA3	AU23		DDRO_D40	AR1	MDA41			
				DDRO_D41	AR4	MDA45			
<->	CSA0	AU14		DDRO_D42	AN2	MDA42			
<->	CSA1	AV9		DDRO_D43	AN1	MDA43			
<->	CSA2	CSA2		DDRO_D44	AR2	MDA44			
<->	CSA3	AW8		DDRO_D45	AR4	MDA40			
				DDRO_D46	AN2	MDA46			
<->	DCLKA0	AY15		DDRO_D47	AN1	MDA47			
<->	DCLKA0	AY16		DDRO_D48	AL1	MDA49			
<->	DCLKA1	AW15		DDRO_D49	AL3	MDA50			
<->	DCLKA1	AW15		DDRO_D50	AJ3	MDA50			
<->	DCLKA2	AW14		DDRO_D51	AJ4	MDA51			
<->	DCLKA2	AW13		DDRO_D52	AL2	MDA52			
<->	DCLKA3	AY13		DDRO_D53	AL3	MDA44			
				DDRO_D54	AJ2	MDA54			
		AW12		DDRO_D55	AJ1	MDA55			
				DDRO_D56	AG1	MDA57			
				DDRO_D57	AG4	MDA61			
				DDRO_D58	AE3	MDA58			
				DDRO_D59	AE4	MDA59			
				DDRO_D60	AG2	MDA60			
				DDRO_D61	AG3	MDA56			
				DDRO_D62	AE1	MDA62			
<->	-SRASA	AW12C		DDRO_RAS*	AE39	DSQA0			
					AJ38	DSQA1			
<->	-SWEA	AW11C		DDRO_WE*	AV36	DSQA2			
					AV35	DSQA3			
		AW20C		DDRO_DOS_P2	AV36	DOSA4			
		AW27C		DDRO_DOS_P3	AP3	DOSA5			
				DDRO_DOS_P4	AP4	DOSA6			
<->	-SCASA	AU9C		DDRO_CAS*	AF3	DSQA7			
					AF2				
<->	-DDR3_RST	WR61	AK22C	DDRO_RESET*	AV32	DSQA0			
		0.1uH/47K/16V/K/X			AE38	DSQA8			
					AN38	DSQA1			
					AN36	DSQA2			
					AN37	DSQA3			
					AW5	DSQA4			
					AP1	DSQA5			
					AK2	DSQA6			
					AF2	DSQA7			
					AF3				
					DDRO_DOS_N0				
					DDRO_DOS_N1				
					DDRO_DOS_N2				
					DDRO_DOS_N3				
					DDRO_DOS_N4				
					DDRO_DOS_N5				
					DDRO_DOS_N6				
					DDRO_DOS_N7				
					DDRO_DOS_N8				

HASWELL/10SC1-F01150-11R_10SC1-F01150-12R]

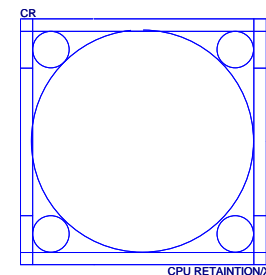
LGA1150 (B)

LGA1150B					
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MAAB1	AK23	DDR1_MA1	DDR1_D01	AE35	MD81
MAAB2	AM22	DDR1_MA2	DDR1_D02	AG35	MD82
MAAB3	AM23	DDR1_MA3	DDR1_D03	AH35	MD83
MAAB4	AP23	DDR1_MA4	DDR1_D04	AD34	MD84
MAAB5	AL23	DDR1_MA5	DDR1_D05	AD35	MD85
MAAB6	AY24	DDR1_MA6	DDR1_D06	AG34	MD86
MAAB7	AY25	DDR1_MA7	DDR1_D07	AH34	MD87
MAAB8	AU26	DDR1_MA8	DDR1_D08	AL34	MD88
MAAB9	AW25	DDR1_MA9	DDR1_D09	AL35	MD89
MAAB10	AP18	DDR1_MA10	DDR1_D010	AK31	MD90
MAAB11	AY26	DDR1_MA11	DDR1_D011	AL31	MD111
MAAB12	AV26	DDR1_MA12	DDR1_D012	AK34	MD112
MAAB13	AR15	DDR1_MA13	DDR1_D013	AK35	MD113
MAAB14	AV27	DDR1_MA14	DDR1_D014	AK32	MD114
MAAB15	AY28	DDR1_MA15	DDR1_D015	AL32	MD115
			DDR1_D016	AK34	MD117
MODT_B0	AM17	DDR1_ODT0	DDR1_D017	AP34	MD121
MODT_B1	AL16	DDR1_ODT1	DDR1_D018	AP31	MD123
MODT_B2	AM16	DDR1_ODT2	DDR1_D019	AN35	MD120
MODT_B3	AK15	DDR1_ODT3	DDR1_D020	AP35	MD116
			DDR1_D021	AN32	MD119
	AM26	DDR1_ECC0	DDR1_D022	AP32	MD122
	AP25	DDR1_ECC2	DDR1_D023	AM29	MD125
	AP26	DDR1_ECC3	DDR1_D025	AM28	MD128
	AL26	DDR1_ECC4	DDR1_D026	AR28	MD127
	AL25	DDR1_ECC5	DDR1_D027	AR28	MD130
	AR26	DDR1_ECC6	DDR1_D028	AL29	MD124
	AR25	DDR1_ECC7	DDR1_D029	AL28	MD129
			AP29	MD126	
			DDR1_D030	AP28	MD131
<-> SBA0	SBA0	DDR1_BA0	DDR1_D031	AR12	MD132
<-> SBA1	SBA1	DDR1_BA1	DDR1_D032	AP13	MD133
<-> SBA2	SBA2	DDR1_BA2	DDR1_D033	AP12	MD134
			DDR1_D034	AL12	MD135
<-> CKEB0	CKEB0	DDR1_CKE0	DDR1_D035	AR13	MD136
<-> CKEB1	CKEB1	DDR1_CKE1	DDR1_D036	AP13	MD137
<-> CKEB2	CKEB2	DDR1_CKE2	DDR1_D038	AM13	MD138
<-> CKEB3	CKEB3	DDR1_CKE3	DDR1_D038	AM12	MD139
			DDR1_D039	AR9	MD145
<-> CSB0	CSB0	DDR1_CS_N0	DDR1_D040	AP9	MD141
<-> CSB1	CSB1	DDR1_CS_N1	DDR1_D041	AR6	MD147
<-> CSB2	CSB2	DDR1_CS_N2	DDR1_D042	AP9	MD143
<-> CSB3	CSB3	DDR1_CS_N3	DDR1_D043	AR10	MD144
			DDR1_D044	AP10	MD140
			DDR1_D045	AR7	MD142
			DDR1_D046	AM9	MD152
<-> DCLKB0	DCLKB0	DDR1_CLK_P0	DDR1_D047	AL9	MD153
<-> DCLKB1	DCLKB1	DDR1_CLK_P1	DDR1_D048	AL9	MD150
<-> DCLKB2	DCLKB2	DDR1_CLK_P2	DDR1_D049	AL7	MD155
<-> DCLKB3	DCLKB3	DDR1_CLK_P3	DDR1_D050	AL10	MD148
<-> DCLKB4	DCLKB4	DDR1_CLK_P4	DDR1_D051	AL10	MD149
<-> DCLKB5	DCLKB5	DDR1_CLK_P5	DDR1_D052	AM6	MD156
<-> DCLKB6	DCLKB6	DDR1_CLK_P6	DDR1_D053	AM7	MD151
<-> DCLKB7	DCLKB7	DDR1_CLK_P7	DDR1_D054	AH6	MD161
<-> DCLKB8	DCLKB8	DDR1_CLK_P8	DDR1_D055	AH7	MD160
<-> DCLKB9	DCLKB9	DDR1_CLK_P9	DDR1_D056	AH7	MD162
<-> SCASB	SCASB	DDR1_CAS*	DDR1_D057	AH6	MD159
	AL120	RSVD	DDR1_D058	AH7	MD163
<-> SRASB	SRASB	DDR1_RS*	DDR1_D059	AJ6	MD156
<-> SWEB	SWEB	DDR1_WAS*	DDR1_D060	AJ7	MD157
	AK16	DDR1_RE*	DDR1_D061	AH7	MD16
			DDR1_D062	AH7	MD162
			DDR1_D063	AF35	DQSB0
<-> VREF_DQA	VREF_DQA	DDR_VREF_DQ0	DDR_VREF_DQ0		
<-> VREF_DQB	VREF_DQB	DDR_VREF_DQ1	DDR_VREF_DQ1		



Place in CPU bottom side

LGA1150 (CR)



CPU RETENTION/

LGA1150_P



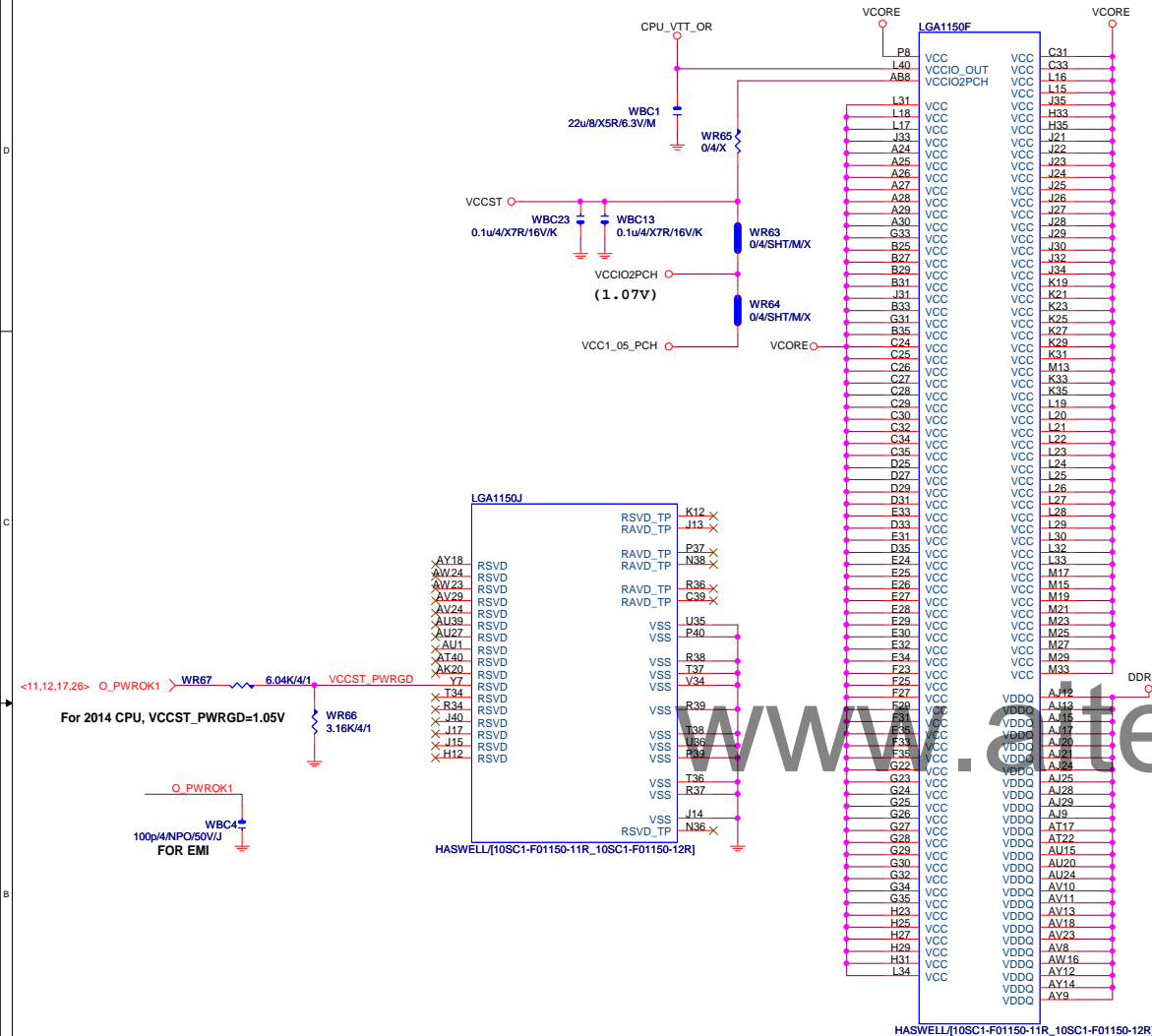
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DDR BUS

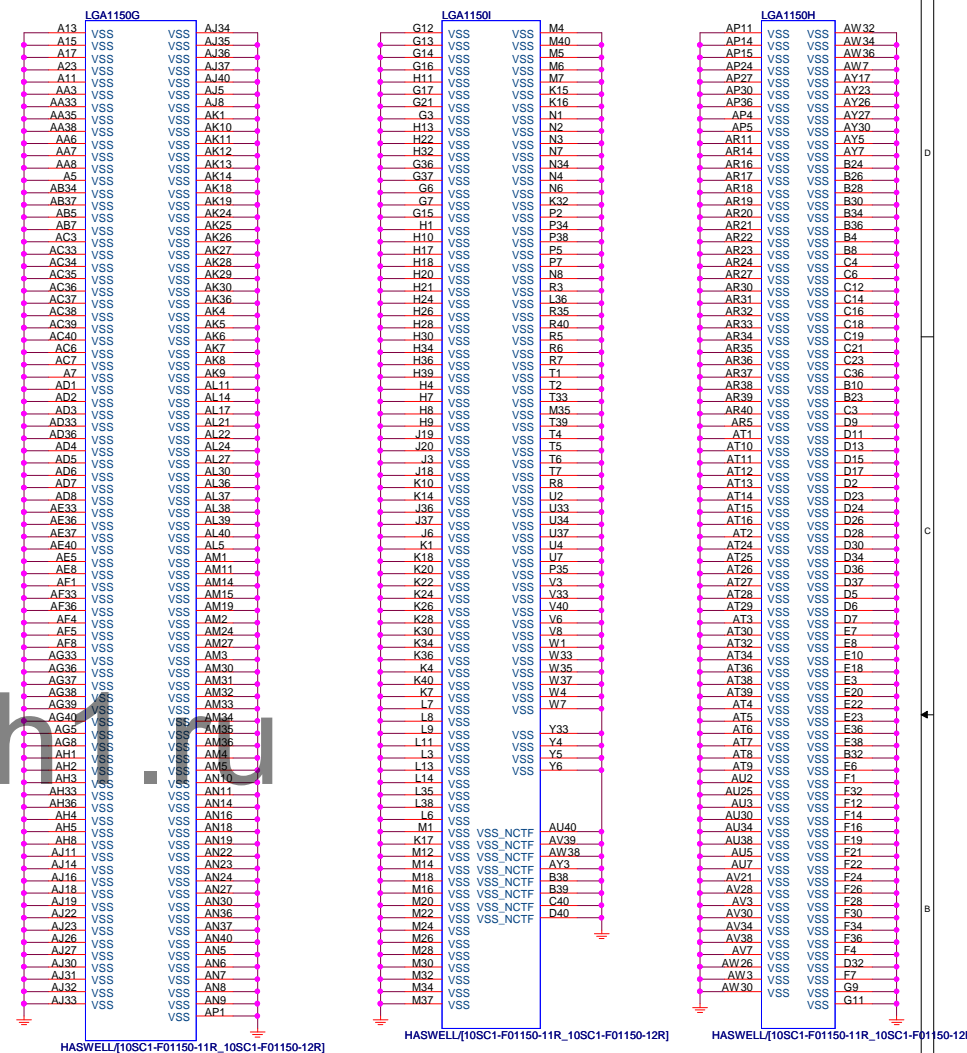
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<8>	MODT_B[0..3]	↔	MODT_B[0..3]
<7>	MDA[0..63]	↔	MDA[0..63]
<8>	MDB[0..63]	↔	MDB[0..63]
<7>	DQSA[0..7]	↔	DQSA[0..7]
<7>	-DQSA[0..7]	↔	-DQSA[0..7]
<7>	MAAA[0..15]	↔	MAAA[0..15]
<8>	MAAB[0..15]	↔	MAAB[0..15]
<8>	DQSB[0..7]	↔	DQSB[0..7]
<8>	-DQSB[0..7]	↔	-DQSB[0..7]

(F, J)

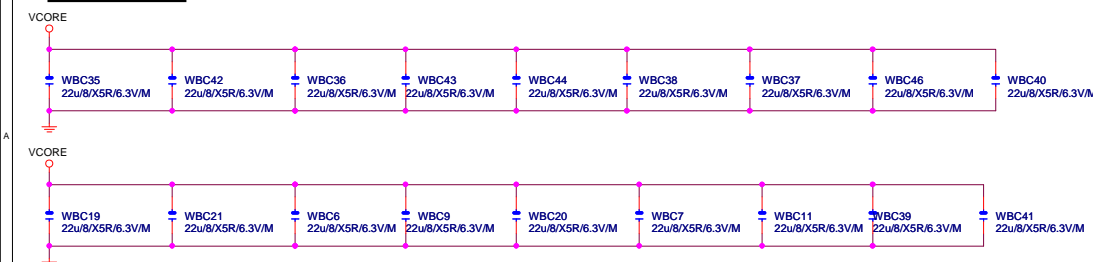
(1.0V)



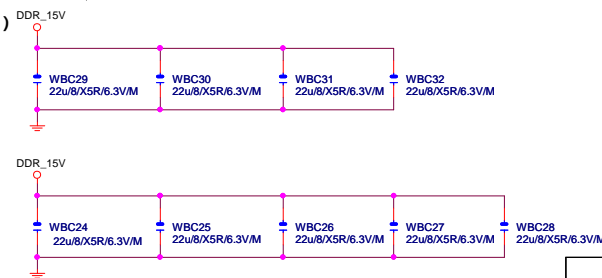
LGA1155 (G,H,I)



VCore CAP (X18)

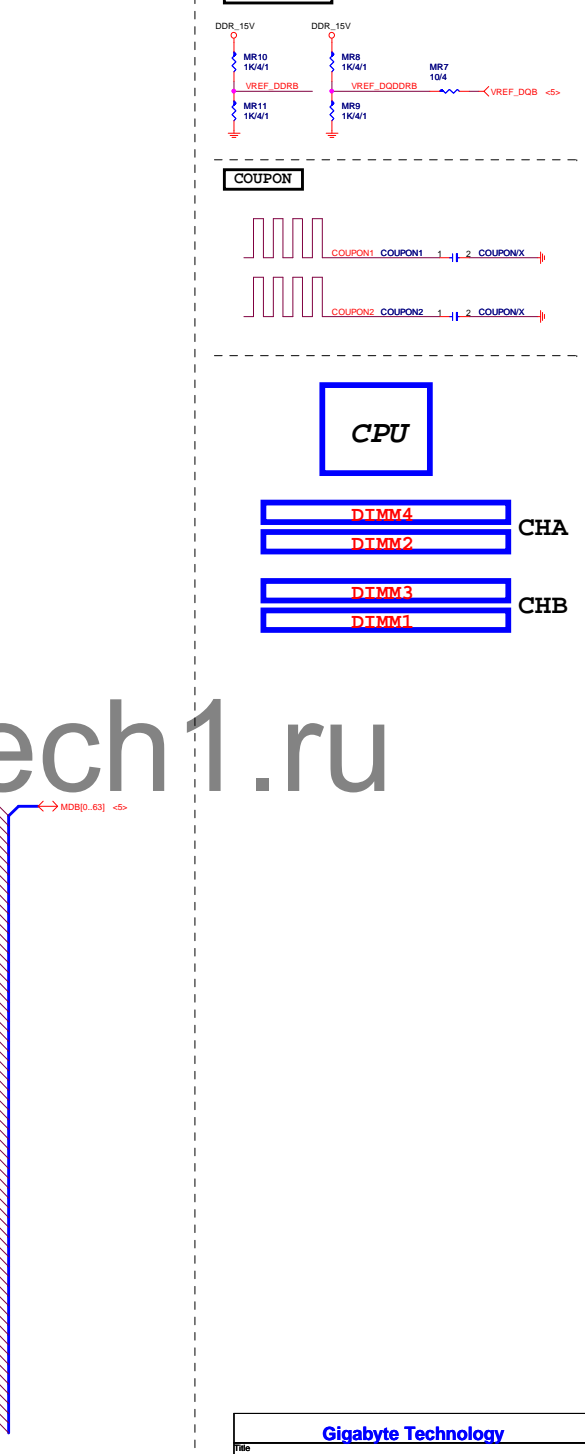
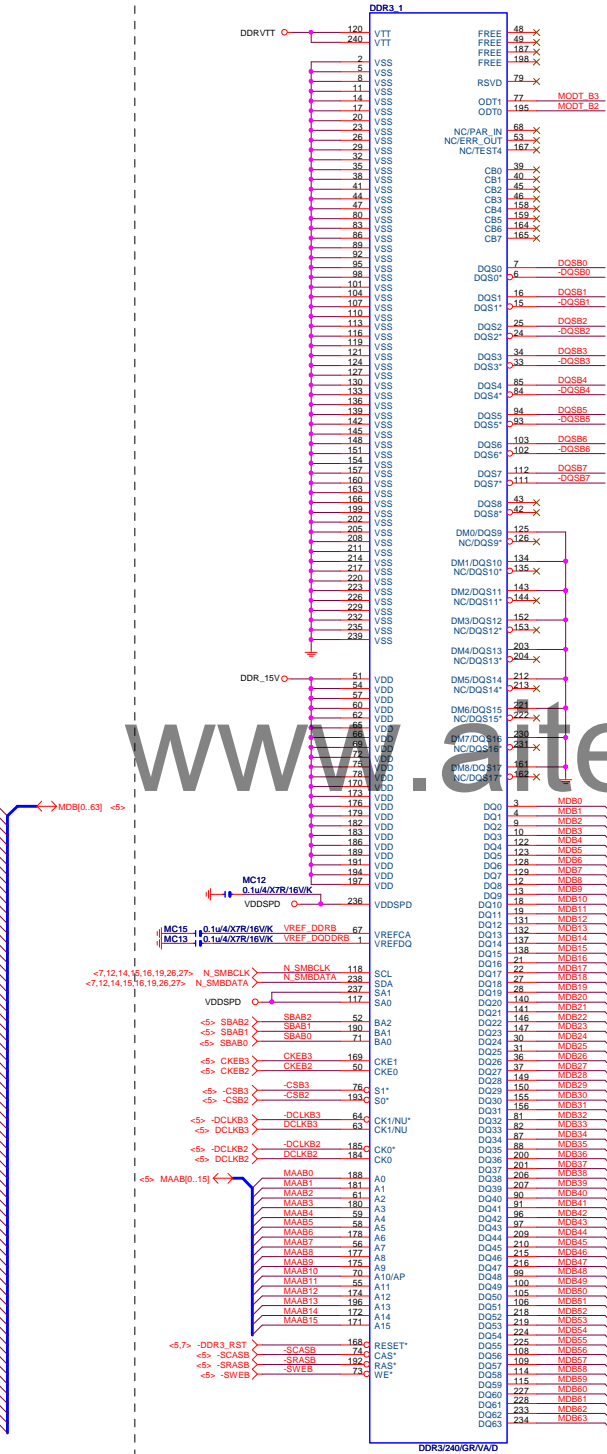
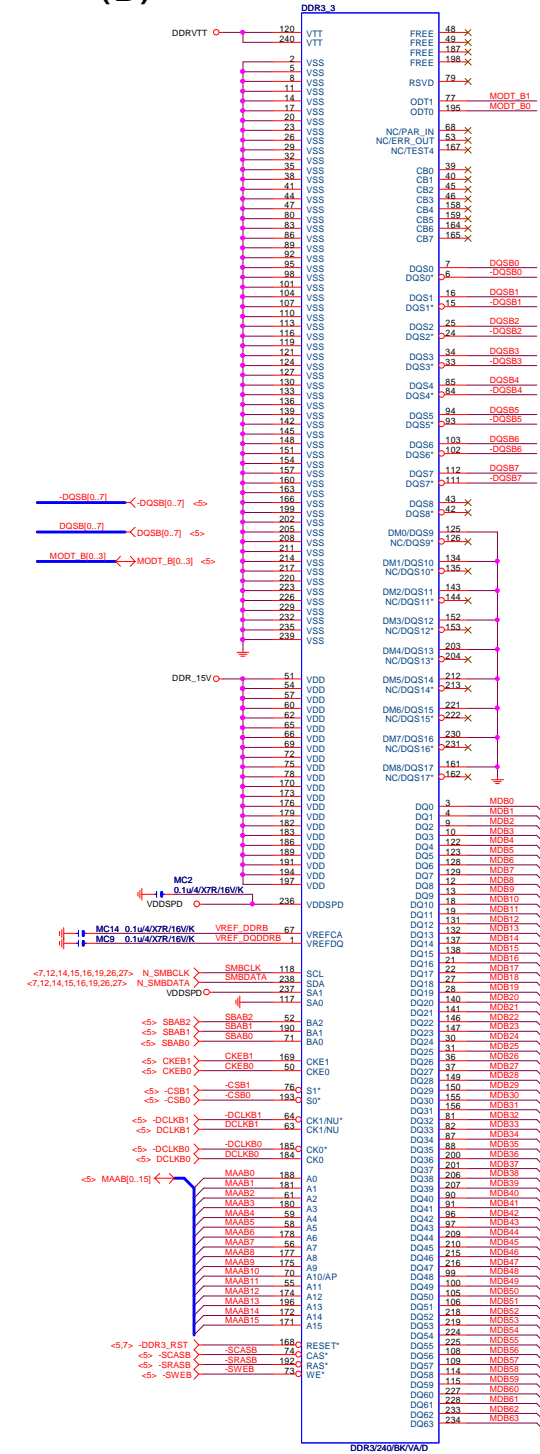


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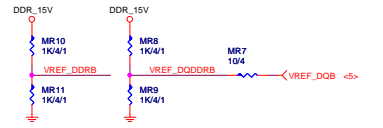


DDR3

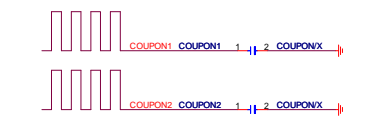
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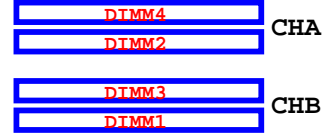
DDR3 VREF



COUPON



CPU



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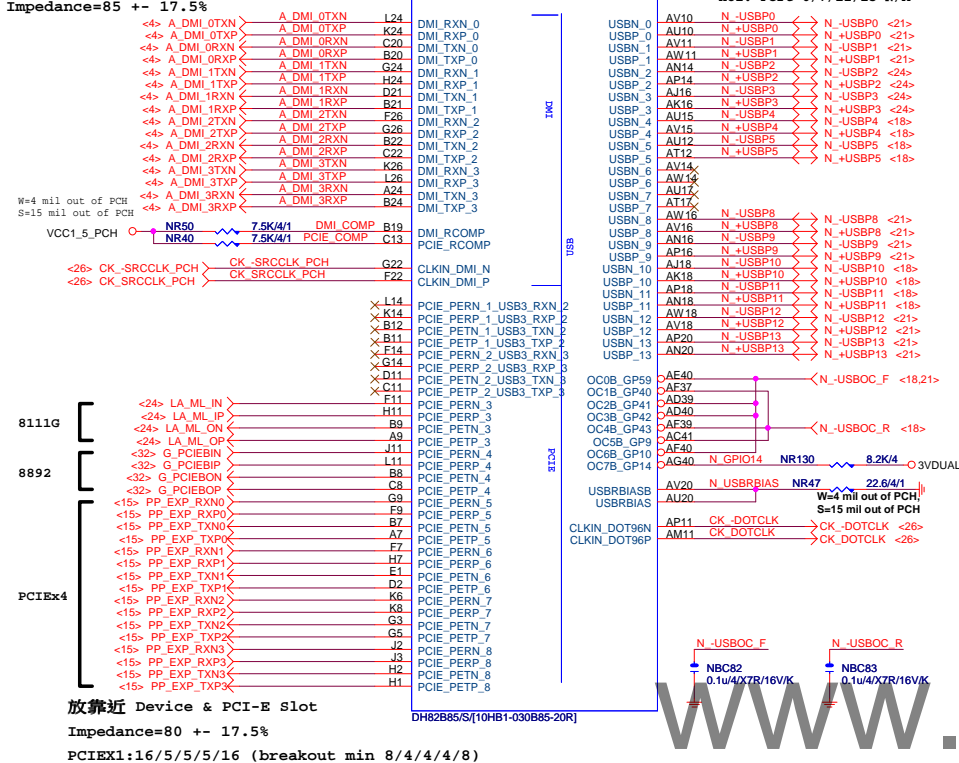
DMI:12/4/4/4/12(breakout min 8/4/4/4/8)
Impedance=85 +- 17.5%

USB2.0 : 12/4.5/7.5/4.5/12 (breakout min 8/4/4/4/8)
Impedance=90 +- 17.5%

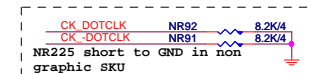
PCHB

B85: Port 6/7 N/A

H81: Port 6/7/12/13 N/A

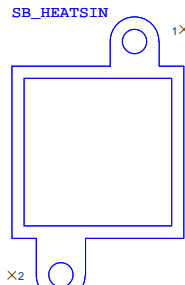
[illegible]

Mount for integrated clock Generation Mode



Pin connection diagram for the DH82B85/S 10HB1-030B85-20R1. The diagram shows a 28-pin connector with pins AT1 through D41. Pins AT1, AT4, AV1, AV2, AV40, AV41, AW40, B40, B41, C41, D1, and D41 are connected to VSS or VSS_NCTF. Pins TP22 through TP2 are connected to U11, U10, A115, AK14, K34, K33, TP15, TP12, TP10, K16, TP9, TP3, TP2, TP5, TP6, TP7, TP8, R4, P5, L5, AC31, AF3, and AV21 respectively. Pins TP22, TP23, TP21, TP14, TP15, TP12, TP10, K16, TP9, TP3, TP2, TP5, TP6, TP7, TP8, R4, P5, L5, AC31, AF3, and AV21 are marked with an 'X' indicating they are not connected.

SB_HEATSIN



PCH_HS
PCH_HS[12SP2-S04209-01R_12SP2-S04209-02R_12SP2-S04209-03R]

```
OC[3:0]# for Device 29 (ports 0-7)
OC[7:4]# for Device 26 (ports 8-13)
```

USB OC# Configure	
OC0#	F_USB30
OC1#	F_USB1
OC2#	F_USB2
OC3#	F_USB3
OC4#	USB_LAN
OC5#	R_USB30
OC6#	KB_MS_USB
OC7#	Not Use

Title			
PCH FDI,DMI,USB ,PCIE,NVRAM			
Size	Document Number		Rev
Custom	GA-B85M-D3H		1.12
Date:	Wednesday, June 18, 2014	Sheet	9 of 32

PCH (G)

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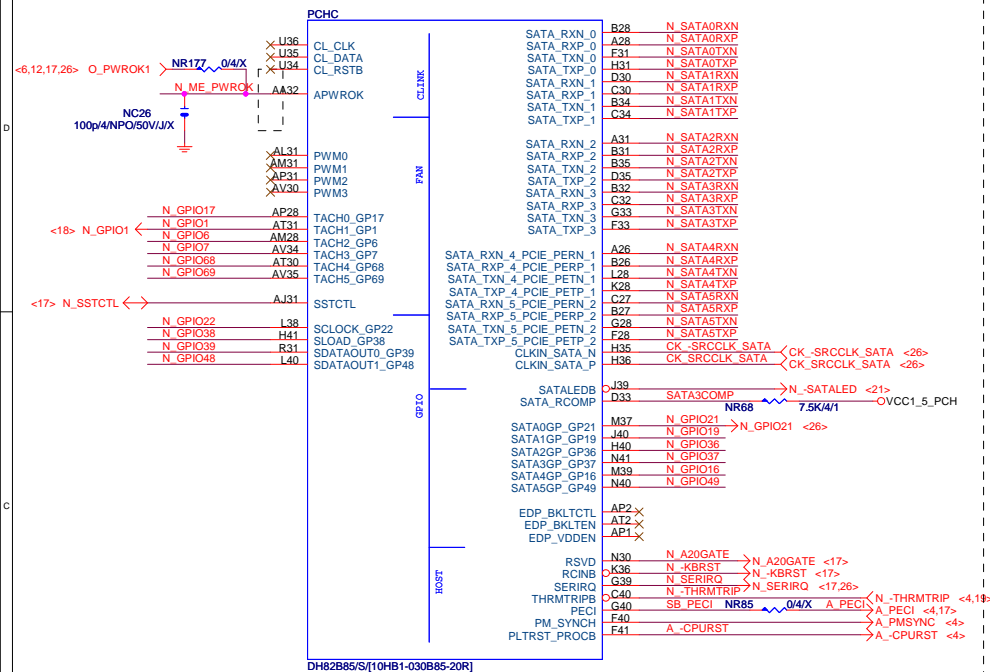
VGA DDC

Gigabyte Technology

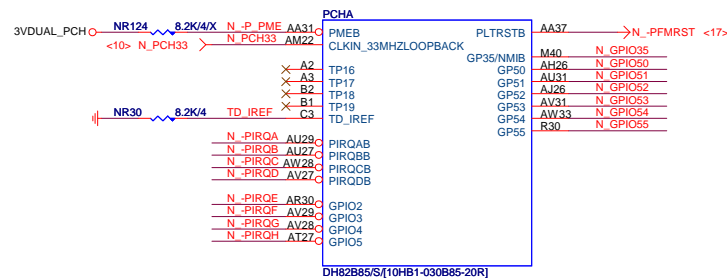
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PCH DISPLAY ,CLK BUFFER			
Size	Document Number	GA-B85M-D3H	Rev
Custom			1.12
Date:	Wednesday, June 18, 2014	Sheet	10 of 32

PCH (C)

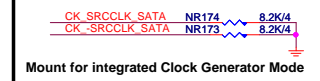
SATA3 : 20/7.5/4.5/7.5/20 (breakout min 8/4/4/4/8)
Impedance=90 +/- 17.5%
SATA2 : 15/7.5/4.5/7.5/15 (breakout min 8/4/4/4/8)
Impedance=90 +/- 17.5%



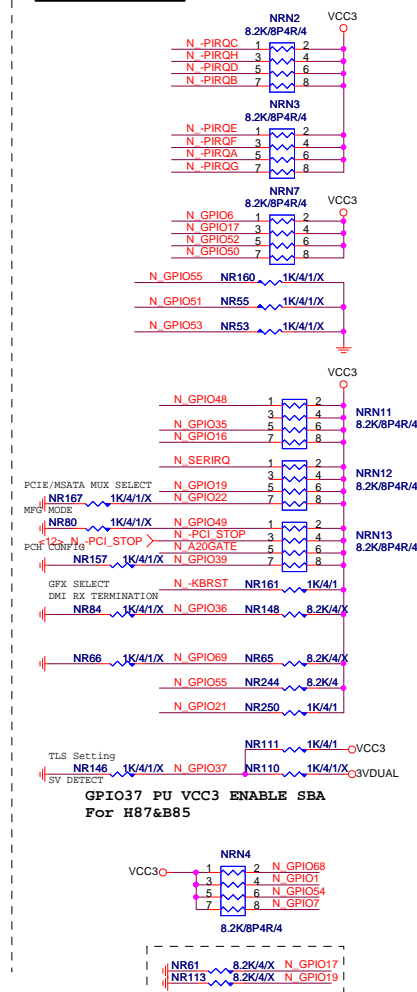
PCH (A)



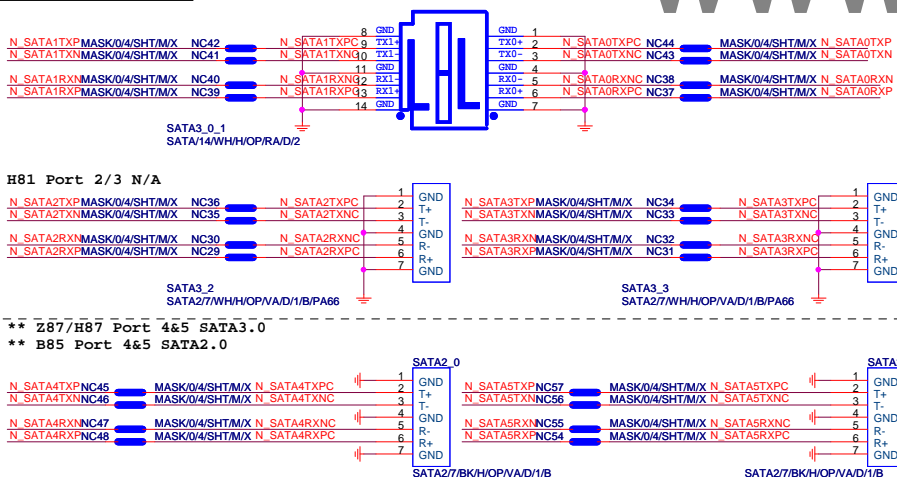
PCH CLK PD



PCH PU/PD

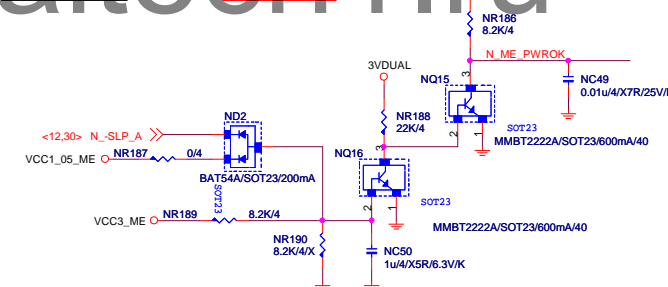


SATA CONNECTOR



ME PWROK

Z87 N/A



(D)



SPI OVERRIDE PROTECTION

At least 10ms delay after 3VDUAL_PCH stable

3VDUAL_PCH

NR69 8.2K

At least 40ns lead fall to 0V before 3VDUAL_PCH fall to 2V

5VSB

NQ4

NR94 22K/4

NQ3

NR116 75K/4/1

NR93 27K/4/1

NC21 1u4/XSR/6.3V/K

NR233 Q/4

NR234 6.19K/4/1/X

NR235 1K/4/1/X

NQ2

NC17 1n4/X7R/50V/K

MMBT2222A/SOT23/600mA/40

MMBT2222A/SOT23/600mA/40

MMBT2222A/SOT23/600mA/40/X

3VDUAL_PCH

The diagram illustrates the 3VDUAL_PCH interface. It shows a central PCH component connected to various N components. The connections are as follows:

- 3VDUAL_PCH** (top) connects to **N_SAR** (NR129, 8.2K/4), **N_GPIO2** (NR60, 8.2K/4), **N_GPIO31** (NR72, 8.2K/4), **N_SLP_LAN** (NR73, 8.2K/4/X), **N_GPIO72** (NR100, 8.2K/4), **N_PCIE_WAKE** (NR76, 1K/4/1), and **N_GPIO23** (NR95, 1K/4/1X).
- VCC3** (top right) connects to **N_GPIO20** (NR109, 1K/4/1), **N_GPIO0** (NR115, 8.2K/4), **N_SYS_RST** (NR164, 8.2K/4), **N_GPIO32** (NR162, 8.2K/4/X), and **N_GPIO33** (NR49, 8.2K/4).
- 3VDUAL** (middle right) connects to **N_PCH_RST** (NR172, 20K/4/1), **N_PCH_ID0** (NR170, 200/4/1), **N_PCH_IDQ** (NR141, 200/4/1), **N_PCH_TMS** (NR168, 200/4/1), and **N_PCH_TCK** (NR87, 200/4/1X).
- 3VDUAL** (bottom left) connects to **N_PCH_RST** (NR143, 1K/4/1X), **N_PCH_ID0** (NR171, 100/4/1), **N_PCH_IDQ** (NR169, 100/4/1), **N_PCH_TMS** (NR142, 100/4/1), **N_PCH_TCK** (NR108, 51/4/1), **N_GPIO18** (NR79, 8.2K/4), **N_GPIO73** (NR134, 8.2K/4), **N_GPIO26** (NR107, 8.2K/4), **N_GPIO25** (NR137, 8.2K/4), **N_SYS_RST** (NC58, 1n/4/X/R/50V/K), and **N_DRAM_PWROK** (NC59, 1n/4/X/R/50V/K).
- 3VDUAL** (bottom left) also connects to **N_LDPCME** (NRN6, 8.2K/BP4/R/4), **N_GPIO06** (NRN6, 8.2K/BP4/R/4), and **N_PCH_HOY** (NRN6, 8.2K/BP4/R/4).
- 3VDUAL** (bottom left) connects to **N_SML1CLK** (NR117, 1K/4/1), **N_SML1DAT** (NR120, 1K/4/1), **N_SML1OBT** (NR122, 499/4/1), **N_SML1CK** (NR123, 499/4/1), **N_SMBCLK** (NR121, 1K/4/1), and **N_SMBDATA** (NR87, 1K/4/1).

NX2-SHT
SHW/D0.64*5.08*6.74

N Y1
N Y2

NR75

10M/4

NX2

32.768K/12.5p/20ppm/TF38/35K/D

N16

18P/4/NPO/50V/J

N18

18P/4/NPO/50V/J

BATTERY-DUAL-4

RB 必須放在BAT外

NR340 0Ω/SHT/M/X

BAT BAT-SK/BK/P/S/D/SN

NR74 1M/4

NR77 20K/4/1

NR78 20K/4/1

NR90 390K/4

NC19 1u4/X5R/6.3V/K

NC15 1u4/X5R/6.3V/K

NC20 1u4/X5R/6.3V/K

VCC3 PEMC1 0.1u4/Y5V/16V/Z

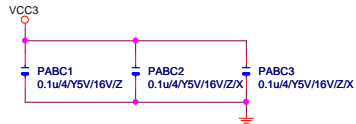
N_RTCVDD <13,19>

N_RTCRST

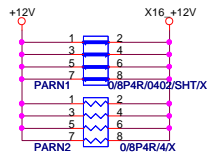
PH1*2/BK/2.54V/A/D

Title			
PCH GPIO, CTRL, AUDIO			
Size	Document Number		Rev
Custom	GA-B85M-D3H		1.12
Date:	Wednesday, June 18, 2014	Sheet	12 of 32

PCIEX16 CAP



PCIEX16 PROTECT SHT

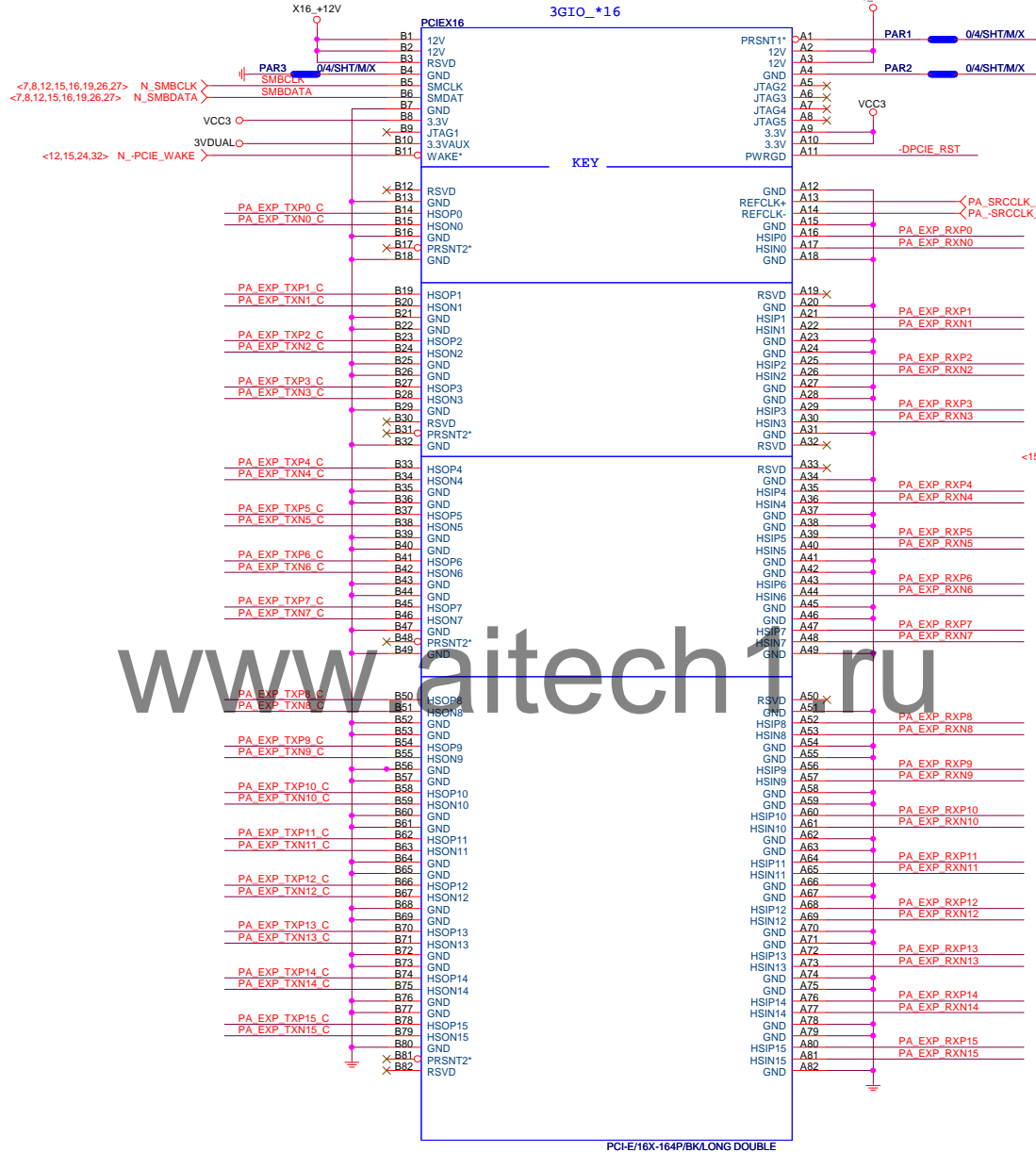


PCIEX16 AC CAP

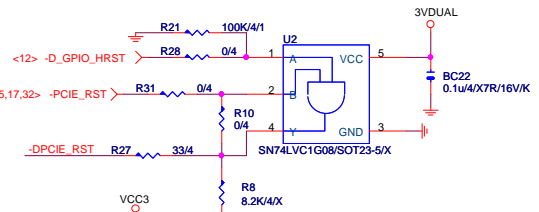
PA EXP TXP0	PAC5	0.22u4/X5R6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u4/X5R6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u4/X5R6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u4/X5R6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u4/X5R6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u4/X5R6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u4/X5R6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u4/X5R6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u4/X5R6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u4/X5R6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u4/X5R6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u4/X5R6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u4/X5R6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u4/X5R6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC18	0.22u4/X5R6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC19	0.22u4/X5R6.3V/K	PA EXP TXN7 C
PA EXP TXP8	PAC20	0.22u4/X5R6.3V/K	PA EXP TXP8 C
PA EXP TXN8	PAC21	0.22u4/X5R6.3V/K	PA EXP TXN8 C
PA EXP TXP9	PAC22	0.22u4/X5R6.3V/K	PA EXP TXP9 C
PA EXP TXN9	PAC23	0.22u4/X5R6.3V/K	PA EXP TXN9 C
PA EXP TXP10	PAC24	0.22u4/X5R6.3V/K	PA EXP TXP10 C
PA EXP TXN10	PAC25	0.22u4/X5R6.3V/K	PA EXP TXN10 C
PA EXP TXP11	PAC26	0.22u4/X5R6.3V/K	PA EXP TXP11 C
PA EXP TXN11	PAC27	0.22u4/X5R6.3V/K	PA EXP TXN11 C
PA EXP TXP12	PAC28	0.22u4/X5R6.3V/K	PA EXP TXP12 C
PA EXP TXN12	PAC29	0.22u4/X5R6.3V/K	PA EXP TXN12 C
PA EXP TXP13	PAC30	0.22u4/X5R6.3V/K	PA EXP TXP13 C
PA EXP TXN13	PAC31	0.22u4/X5R6.3V/K	PA EXP TXN13 C
PA EXP TXP14	PAC32	0.22u4/X5R6.3V/K	PA EXP TXP14 C
PA EXP TXN14	PAC33	0.22u4/X5R6.3V/K	PA EXP TXN14 C
PA EXP TXP15	PAC34	0.22u4/X5R6.3V/K	PA EXP TXP15 C
PA EXP TXN15	PAC35	0.22u4/X5R6.3V/K	PA EXP TXN15 C

PA EXP RXP[0..15] >>> PA_EXP_RXP[0..15] <4>
PA EXP RXN[0..15] >>> PA_EXP_RXN[0..15] <4>
PA EXP TXP[0..15] >>> PA_EXP_TXP[0..15] <4>
PA EXP TXN[0..15] >>> PA_EXP_TXN[0..15] <4>

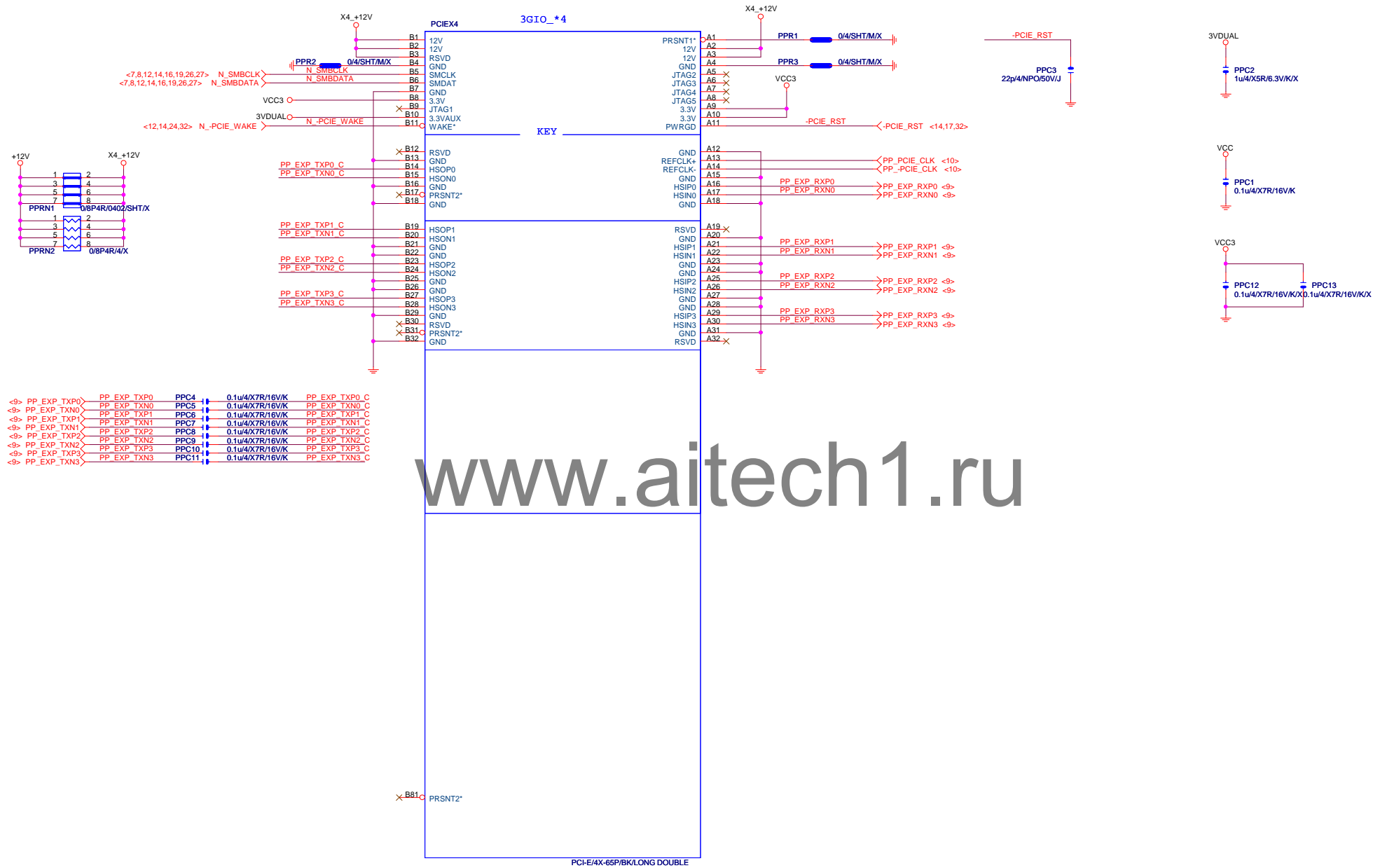
PCIEX16 SLOT



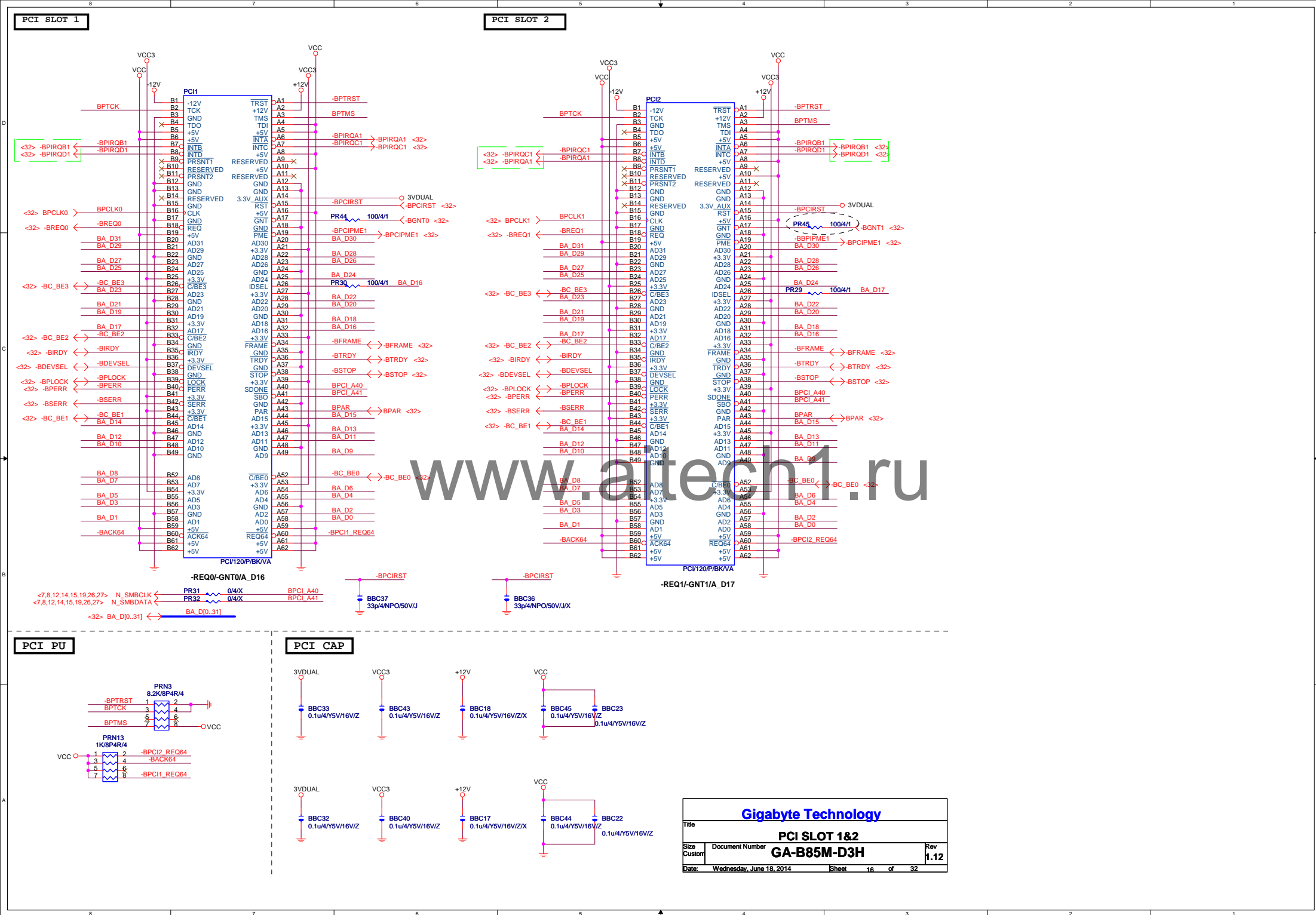
The auxiliary reset circuit is only required for PCIe Gen3 margining and functional link training



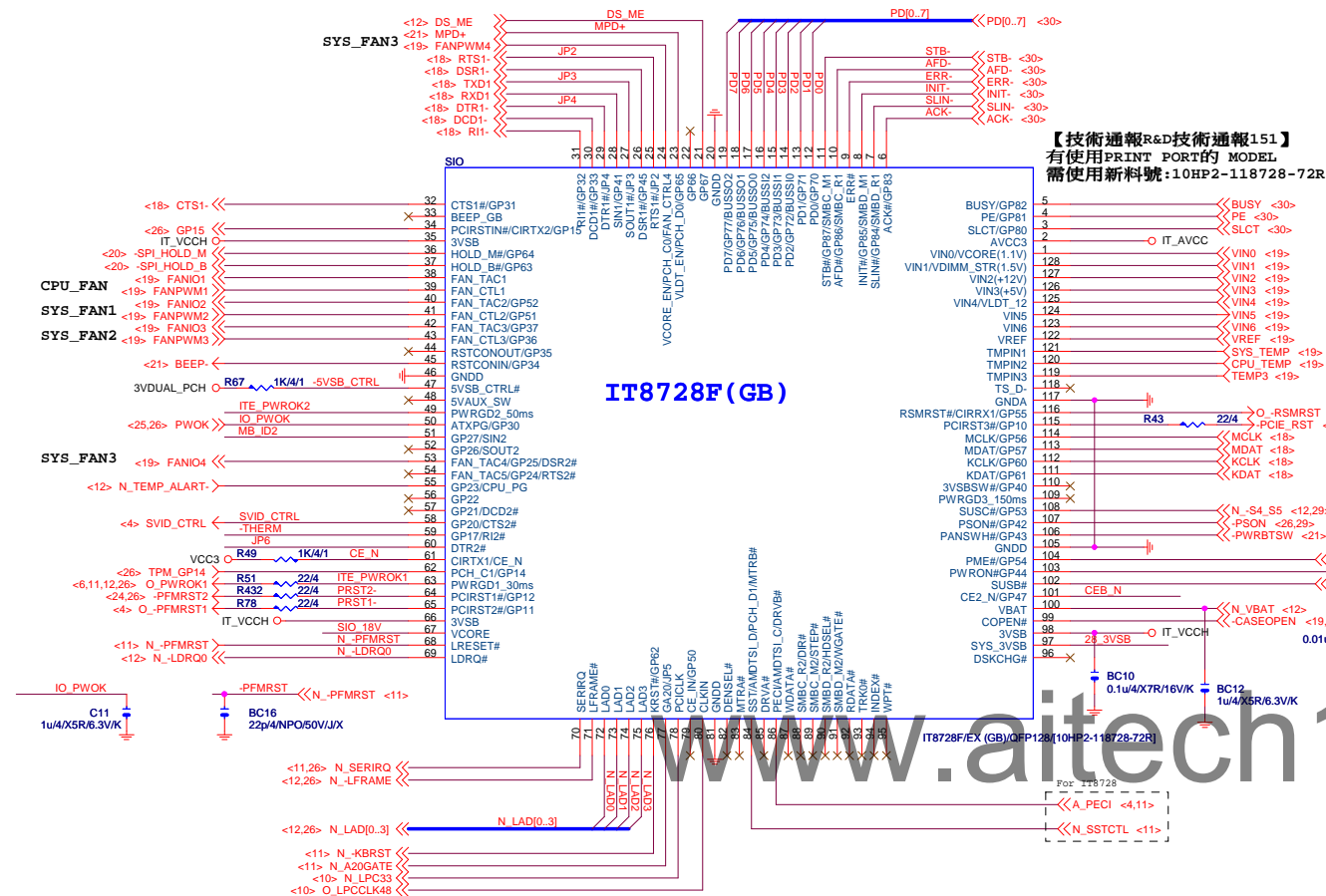
PCIEX4 SLOT



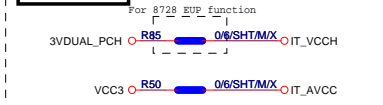
www.aitech1.ru



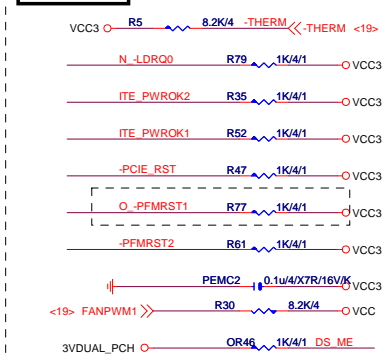
SIO IT8728F



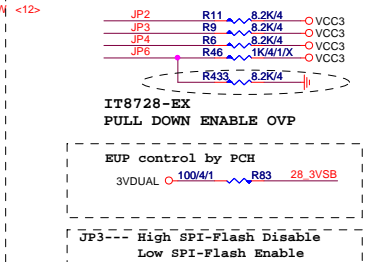
PWR SHT



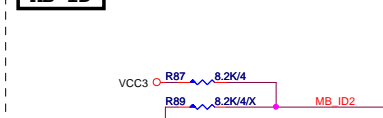
SIO PU



SIO STRAP



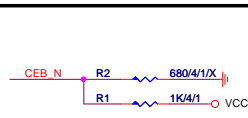
MB ID



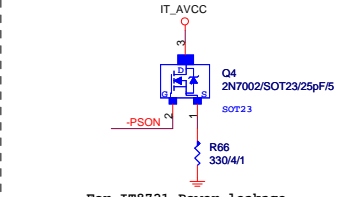
IT8728F NOTE

	IT8728
PIN121	VCORE_EN/PCH_C0
PIN120	VLDI_EN/PCH_D0
PIN19	ATXPG
PIN31	PCH_C1
PIN53	SST/AMDTSLI_D/MTRB# /PCH_D1
PIN55	PECI/AMDTSLI_C/DRV#
PIN66	SYS_3VSB
PIN70	GP47
PIN95	VIN2(VCC5)
PIN96	VIN1(VCC12)
PIN97	VIN1/VDIMM_STR(1.5V)
PIN98	VIN0/VCORE(1.1V)/NC

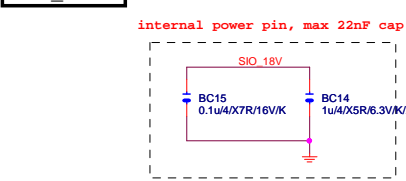
DUAL BIOS OPT STRAP



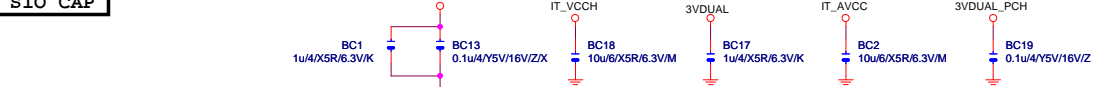
Power leakage

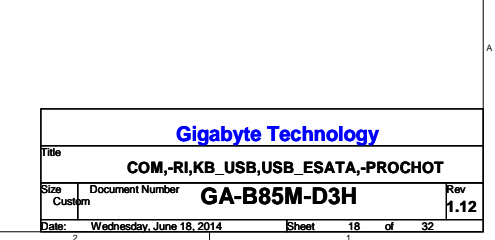
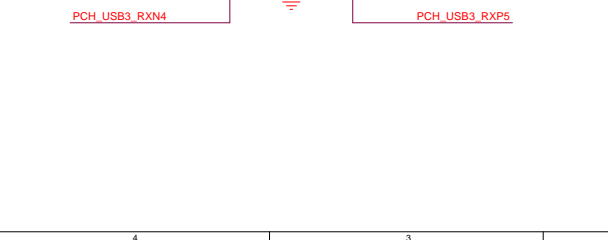
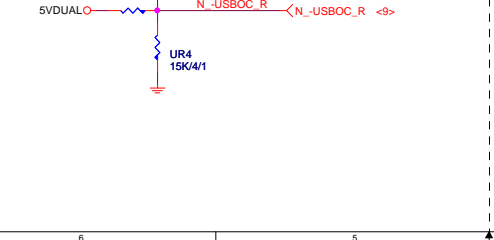
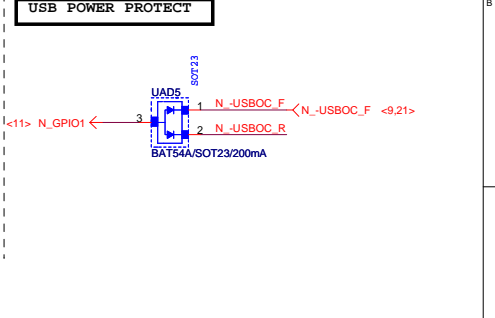
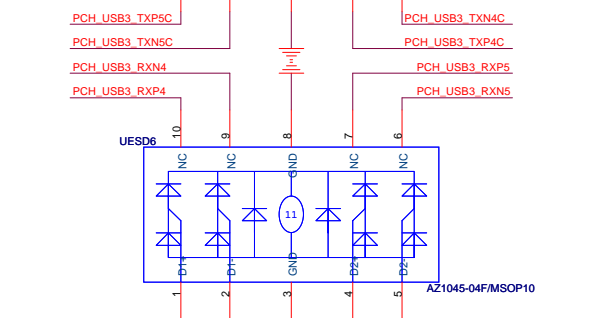
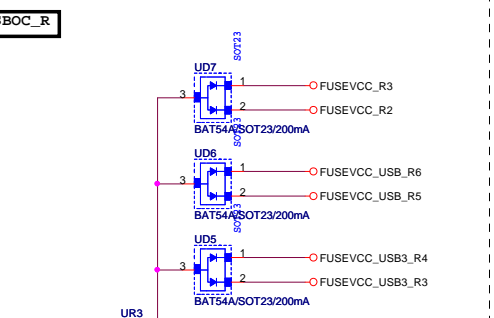
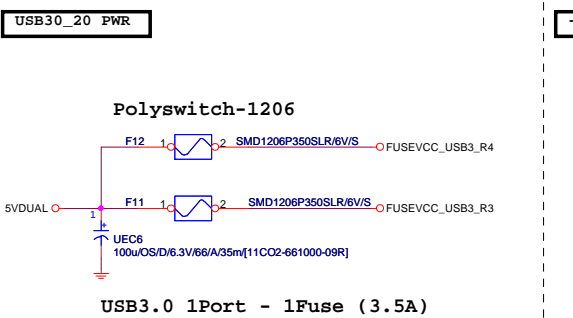
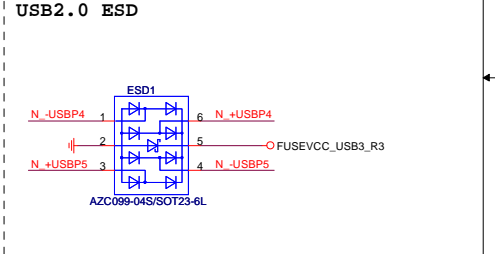
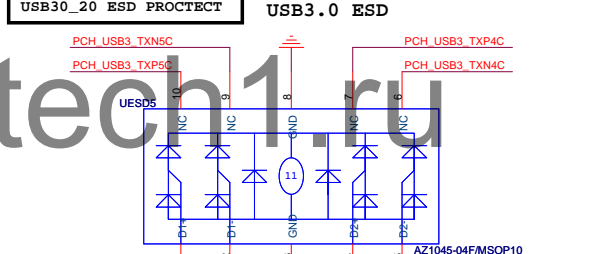
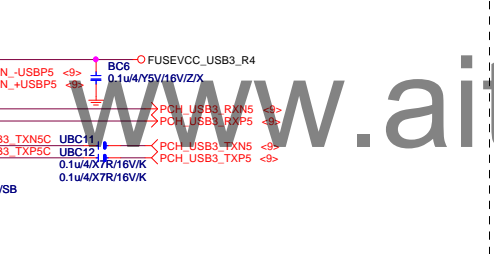
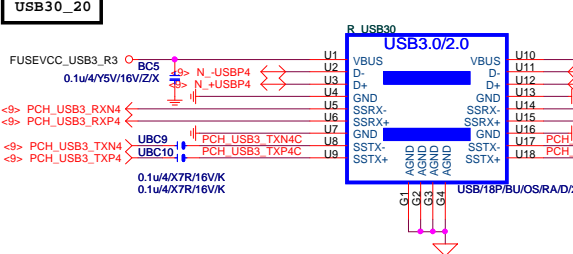
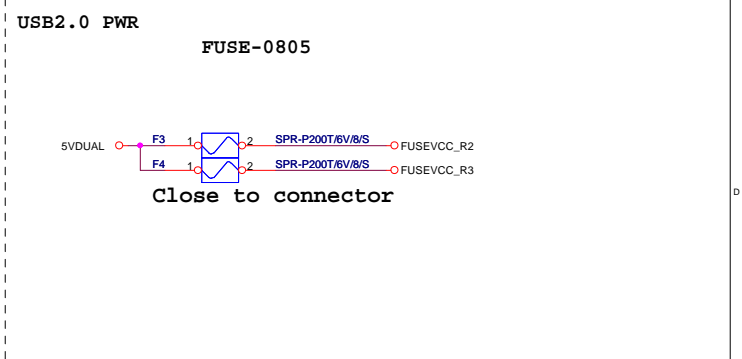
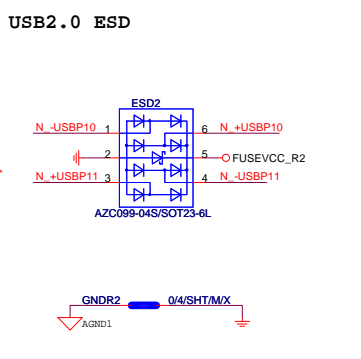
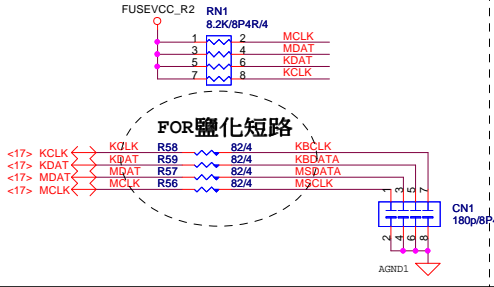
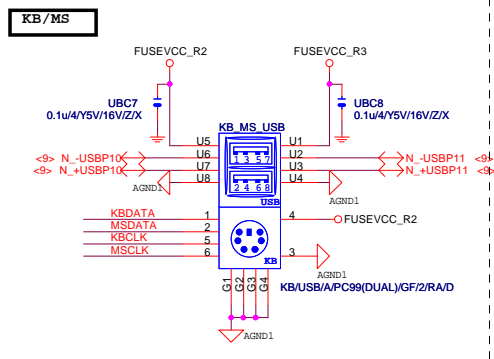
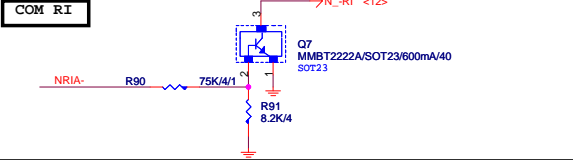
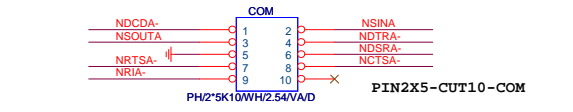
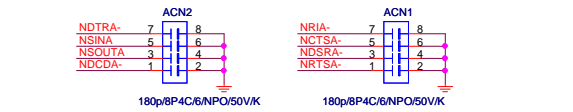
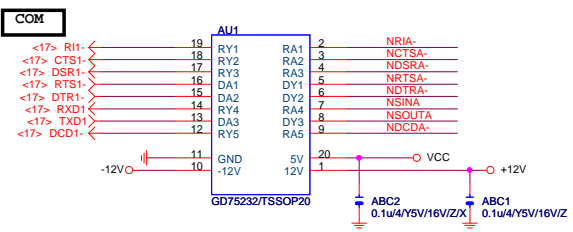


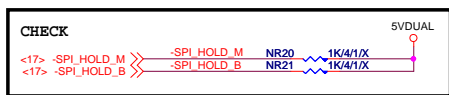
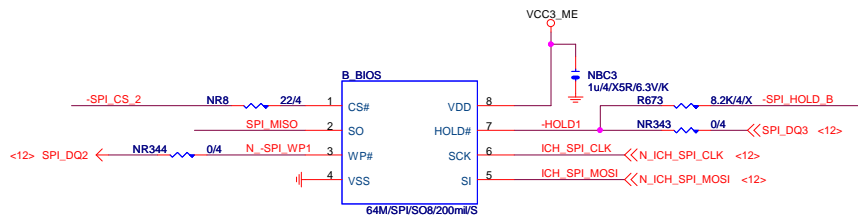
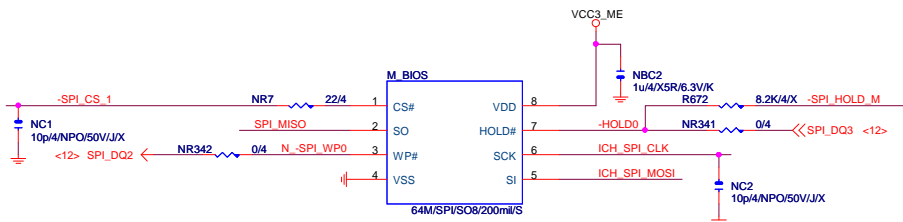
SIO_18V



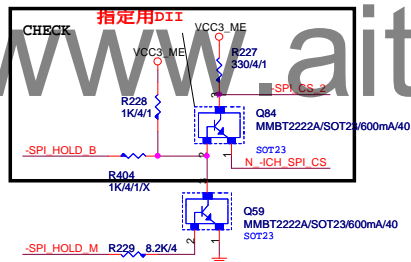
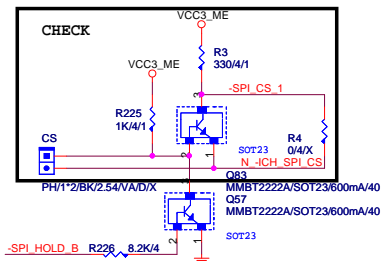
SIO CAP





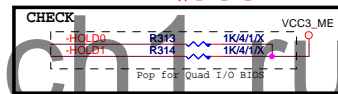
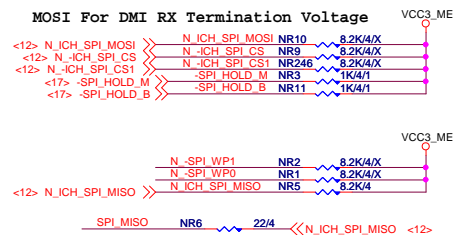


Dual BIOS CS connect
circuit update



BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

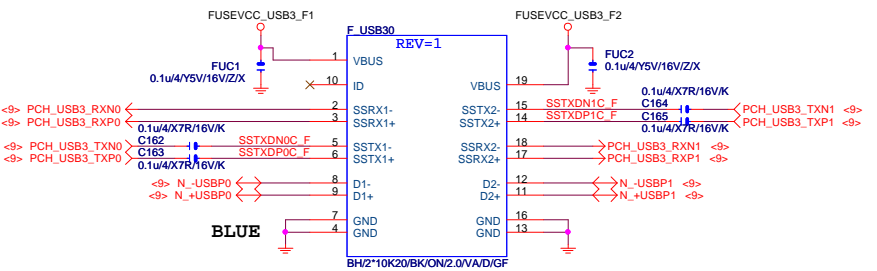
1 means floating
0 means PD 1k



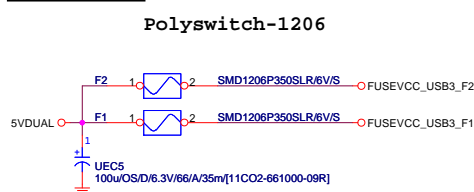
Gigabyte Technology

Title		
DUAL BIOS		
Size	Document Number	Rev
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Date:	Wednesday, June 18, 2014	Sheet 20 of 32

F_USB30

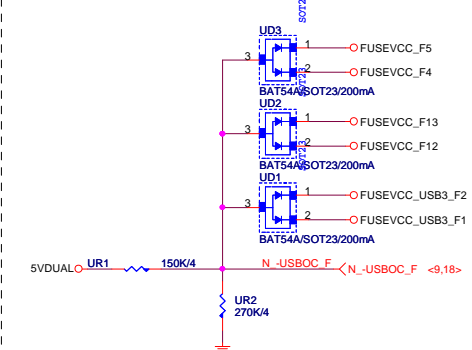


F_USB30 PWR

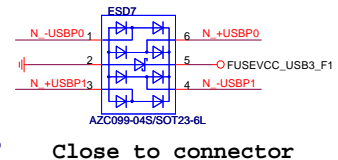
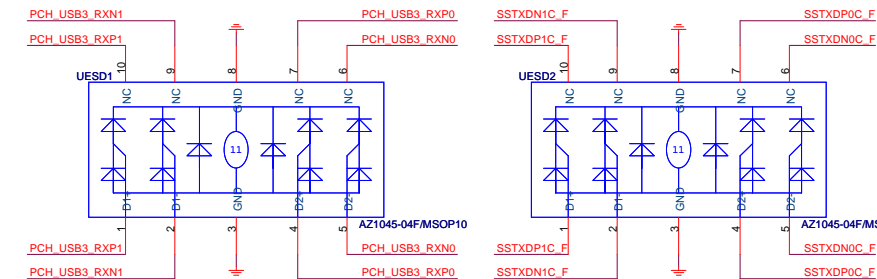


USB3.0 1Port - 1Fuse (3.5A)

-USBOC_F

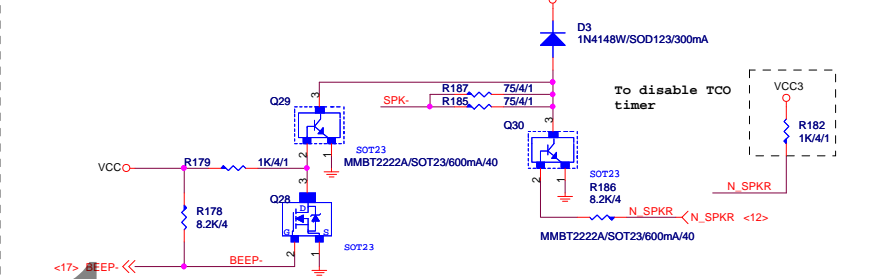


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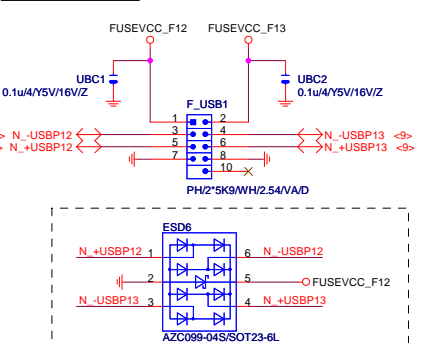


Close to connector

SPKR

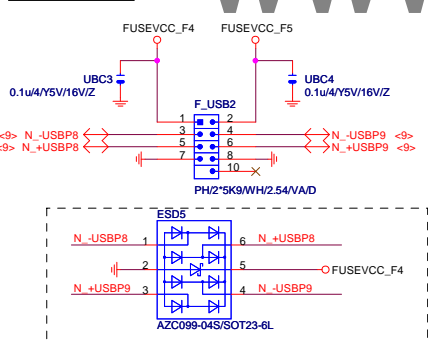


FRONT USB1



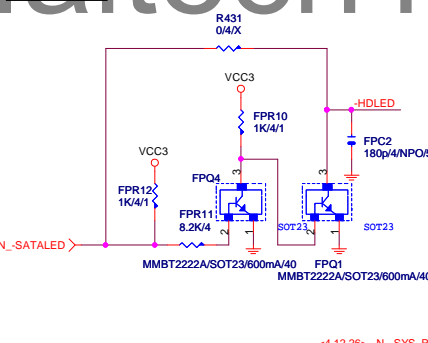
Close to connector

FRONT USB2



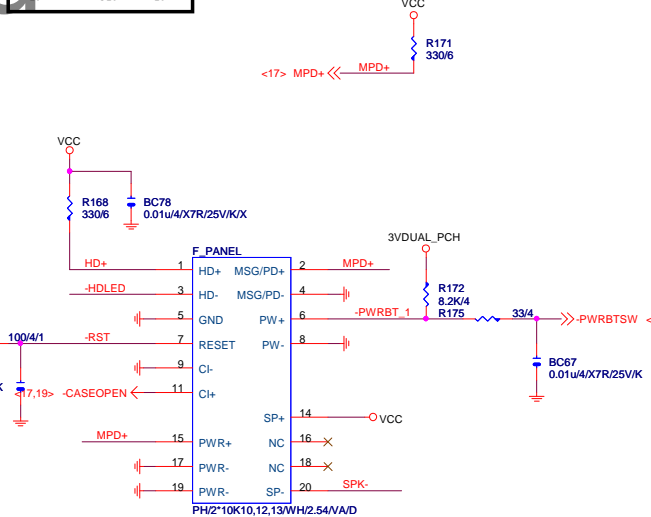
Close to connector

SATA LED

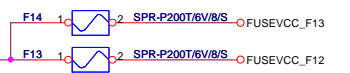


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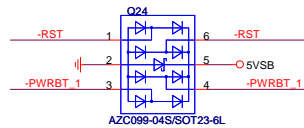
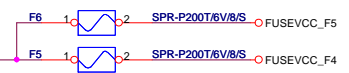
INTEL FRONT PANEL



FUSE-0805



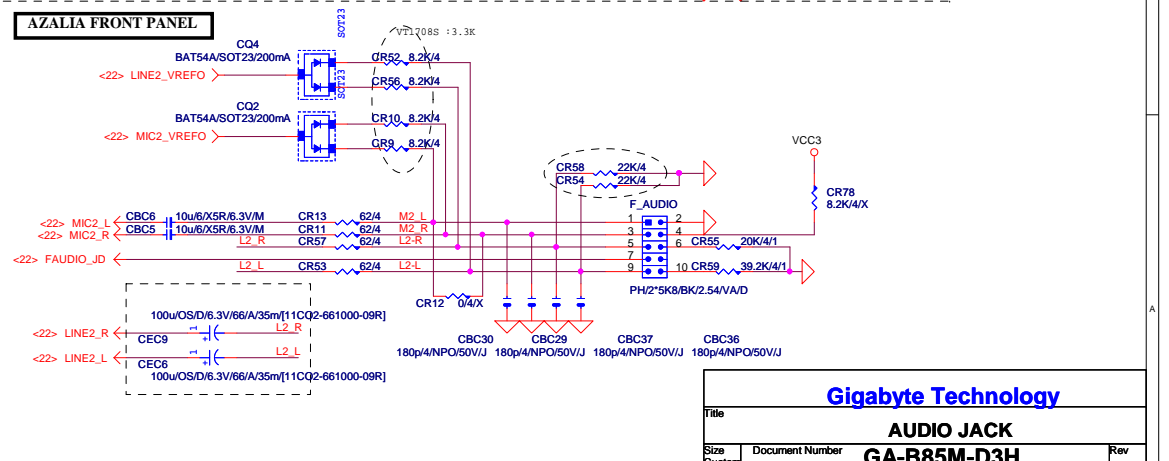
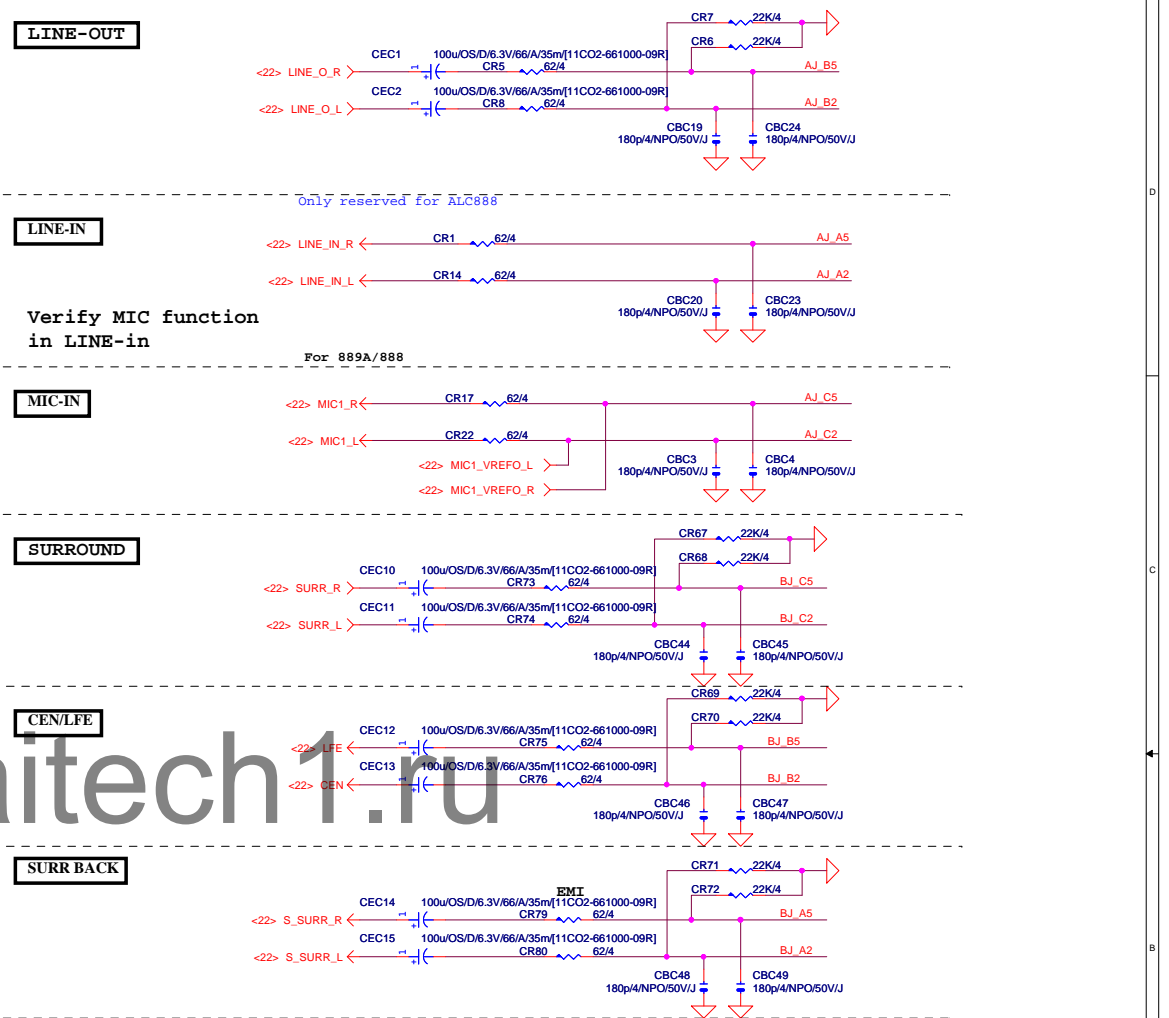
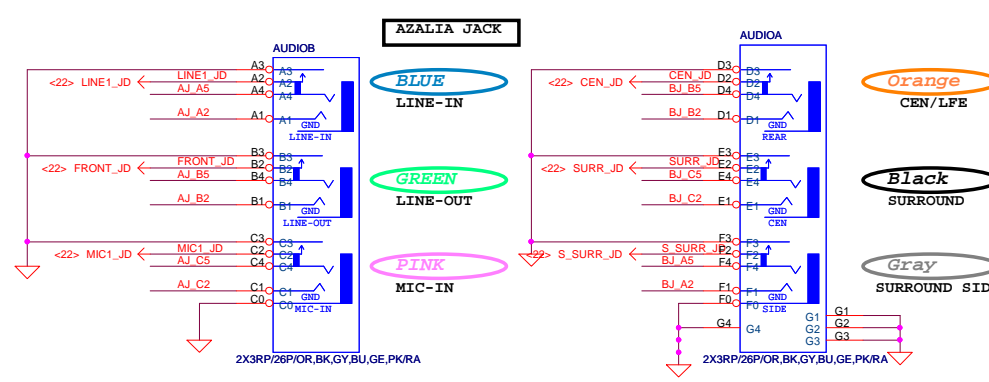
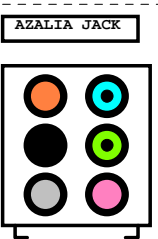
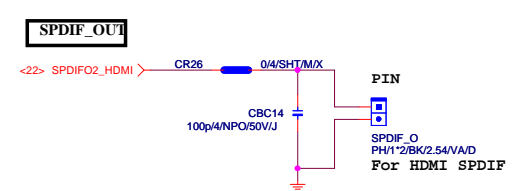
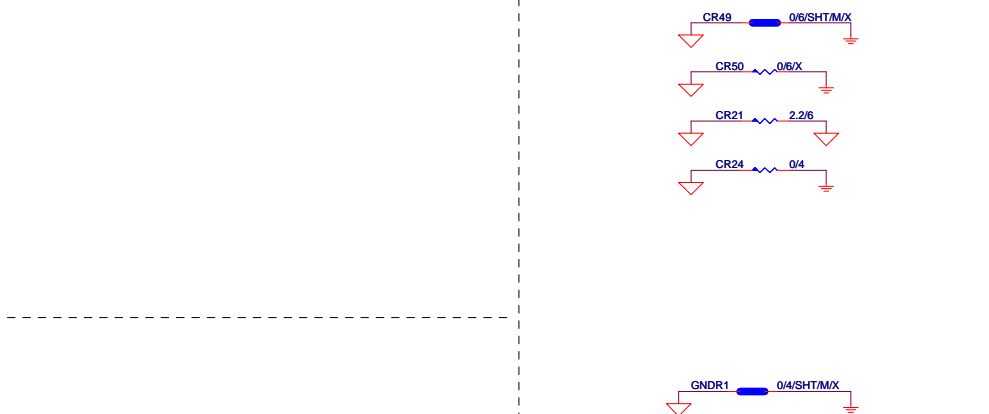
FUSE-0805



Gigabyte Technology			
Title	FP,F_USB,USB PWR,SPKR,SATA LED		
Size	Document Number	GA-B85M-D3H	
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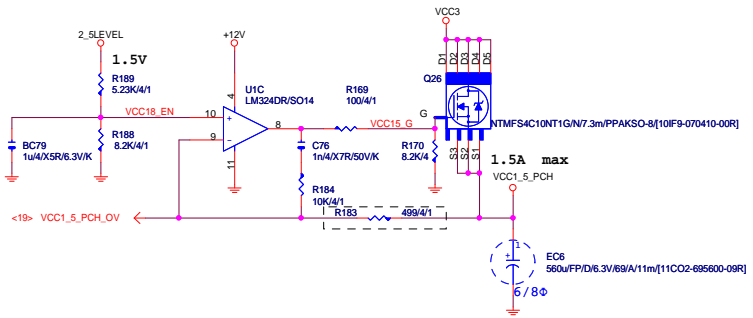
ALC892/ALC887-VD2/VT1708-CE Colay



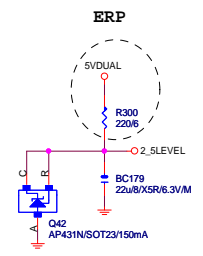


Gigabyte Technology			
AUDIO JACK			
GA-B85M-D3H			
Title	Document Number	Rev	1.12
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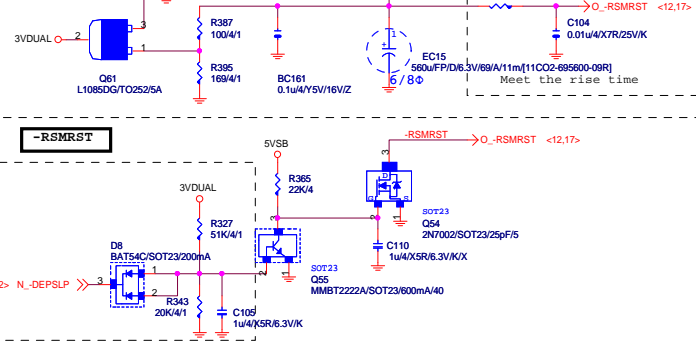
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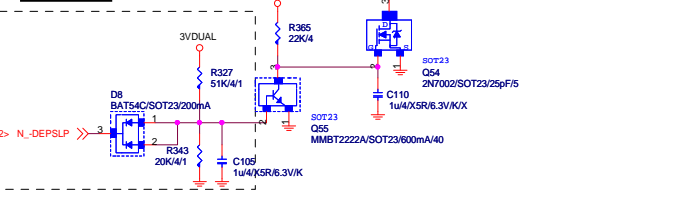
2_5LEVEL



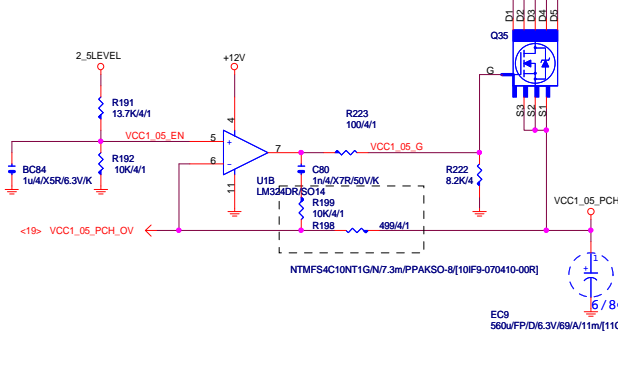
3VDUAL



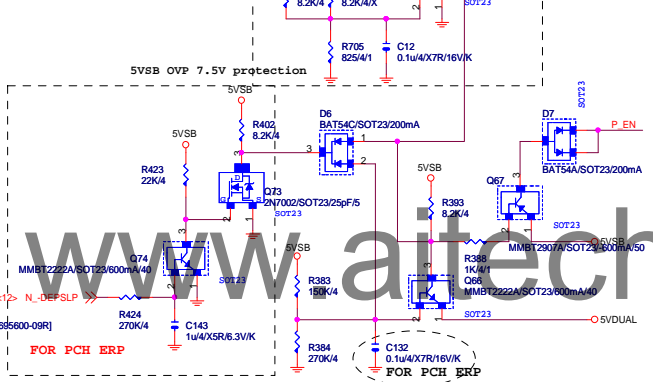
-RSMRST



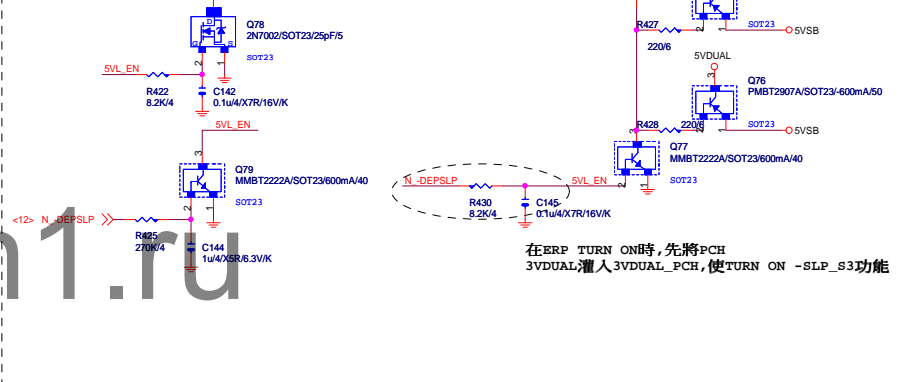
VCC1_05_PCH



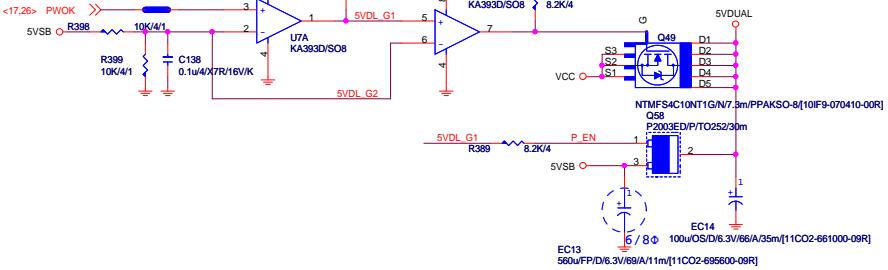
5VDUAL SHORT PROTECT



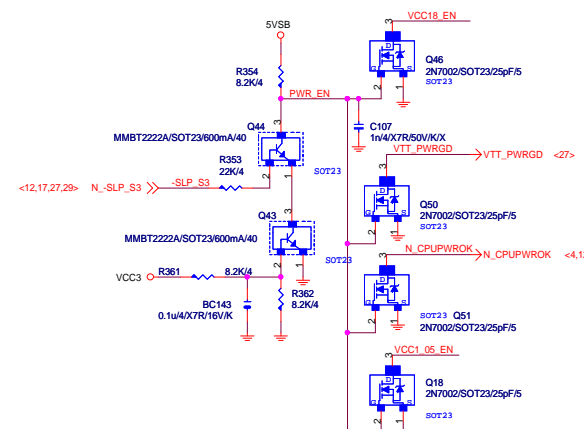
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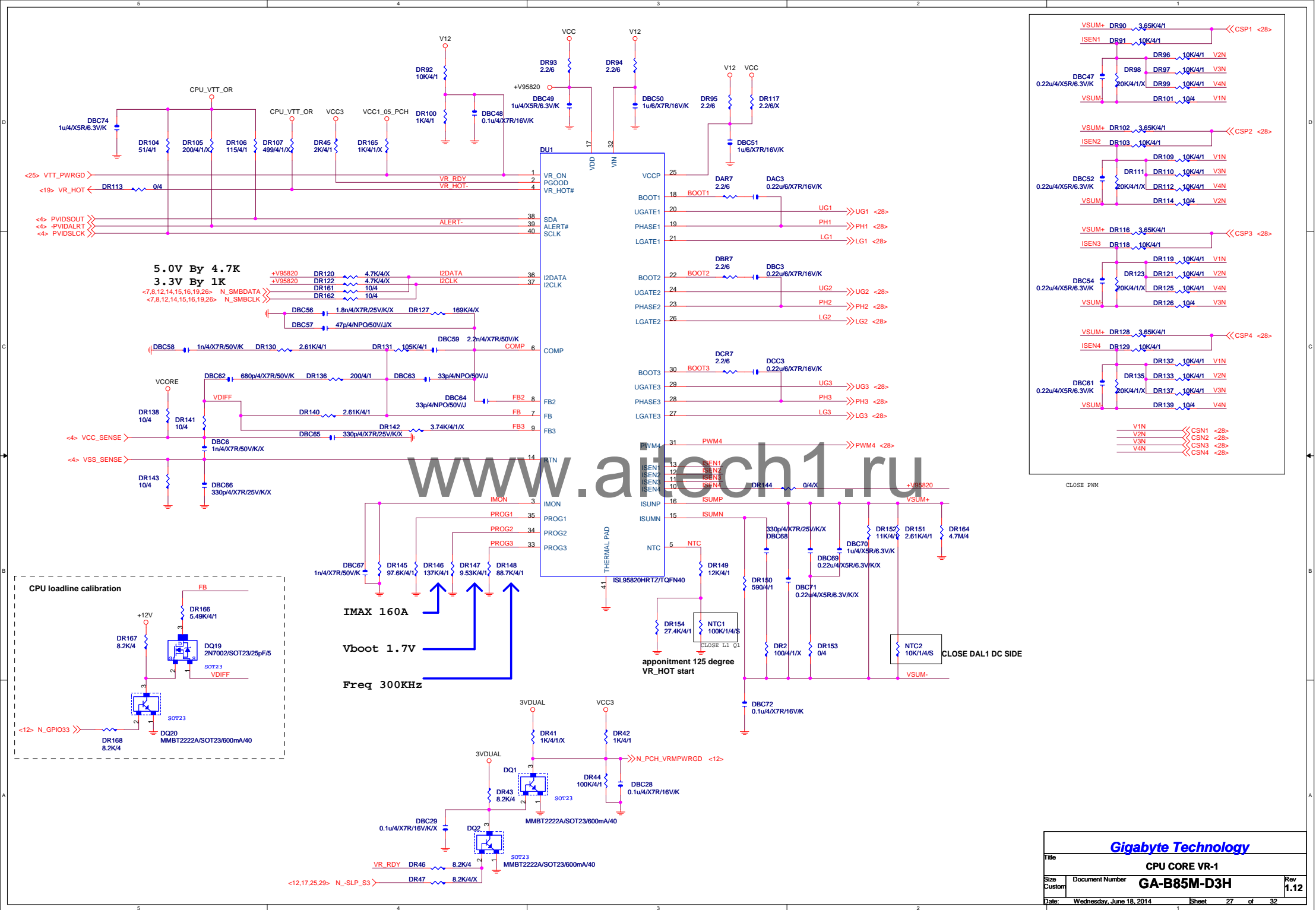


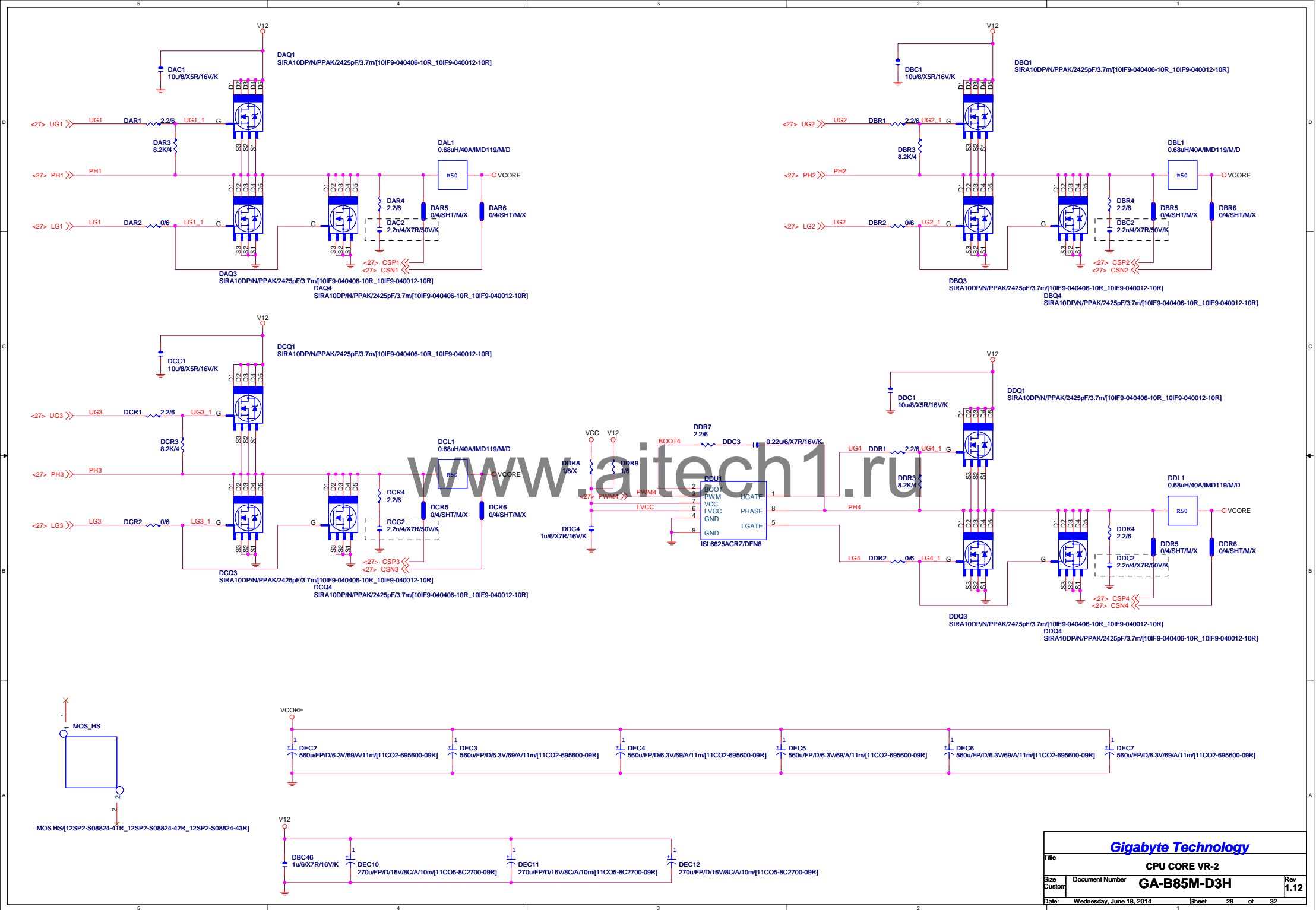
5VDUAL



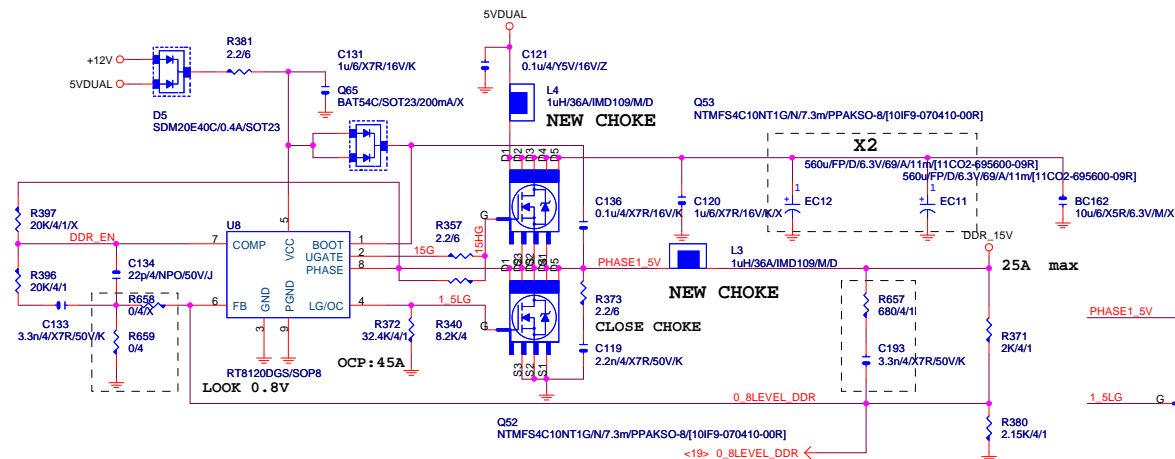
PWR SEQ



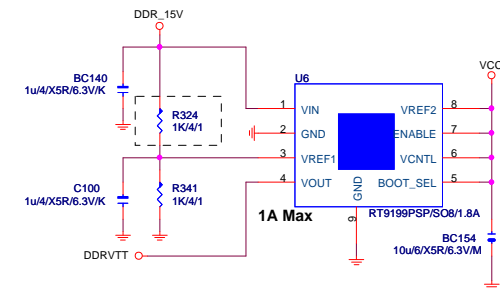




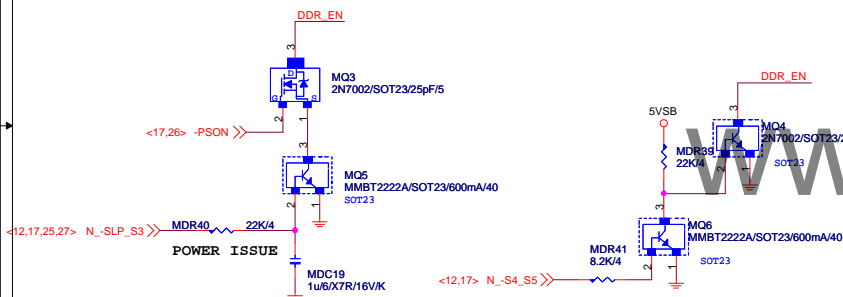
DDR15V



DDRVRTT



PWR SEQ



VIN=5V, VOUT=1.5V, IOUT=25A, PHASE=1

IRMS=11.45A

560u/FP/D/6.3V/68/8m RIPPLE CURRENT=4.7A

Coefficient=1.7(85°C), 1(105°C)

VIN Ripple current=4.7X1.7=7.99A(85°C)

-->故固态电容须2X7.99=15.98>11.45A

$R_{ocset} = (I_{ocp} \cdot L_{gate} + r_{dson}) / I_{ocset}$

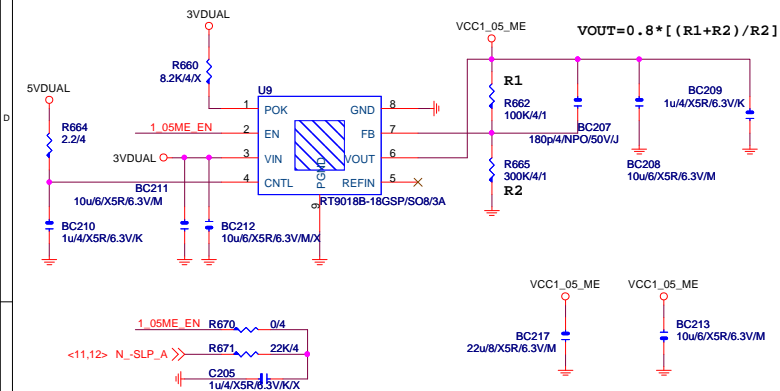
$R_{ocset} = (45A \cdot 6.7m\Omega + 10\mu A) / 10\mu A = 30K$

Iocset=10uA

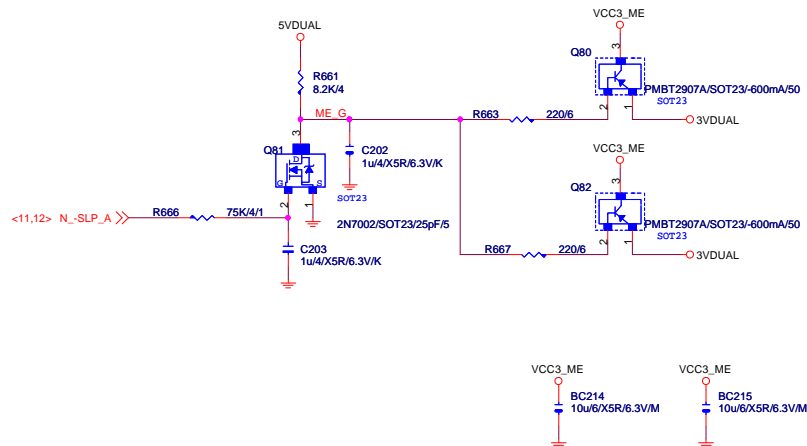
Gigabyte Technology

DDR POWER			
Title	DDR POWER		
Size	Document Number	GA-B85M-D3H	Rev 1.12
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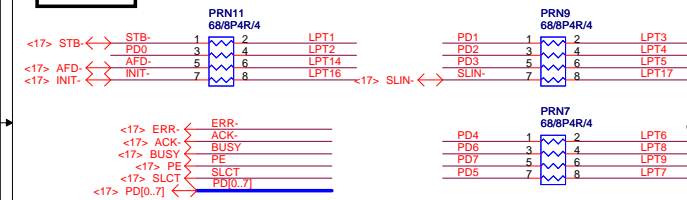
VCC1_05_ME



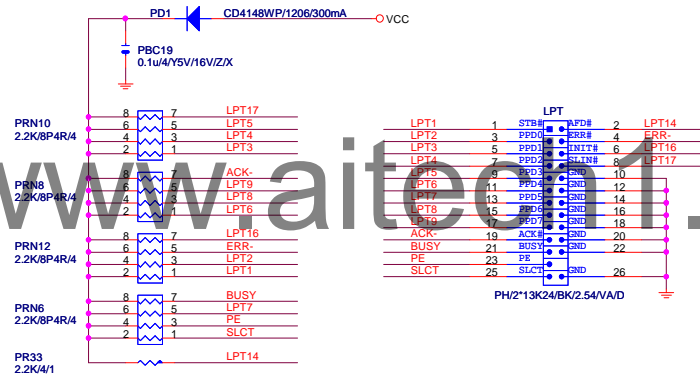
VCC3_ME



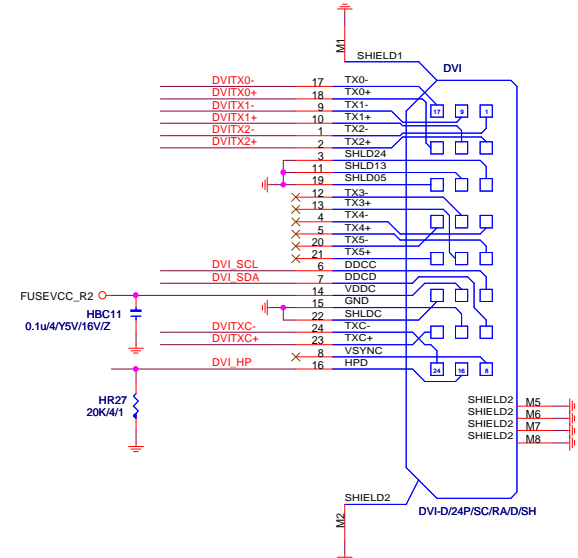
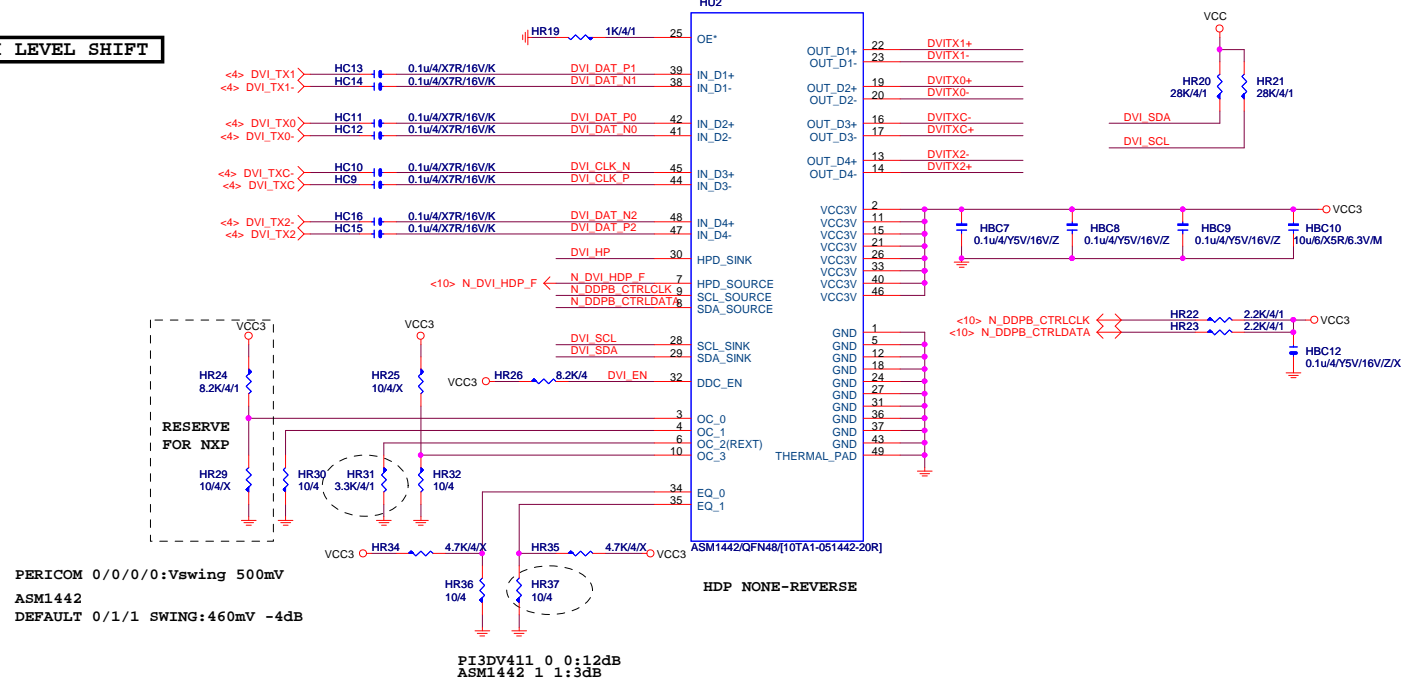
LPT PORT



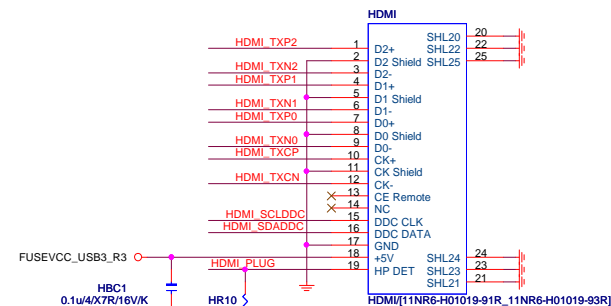
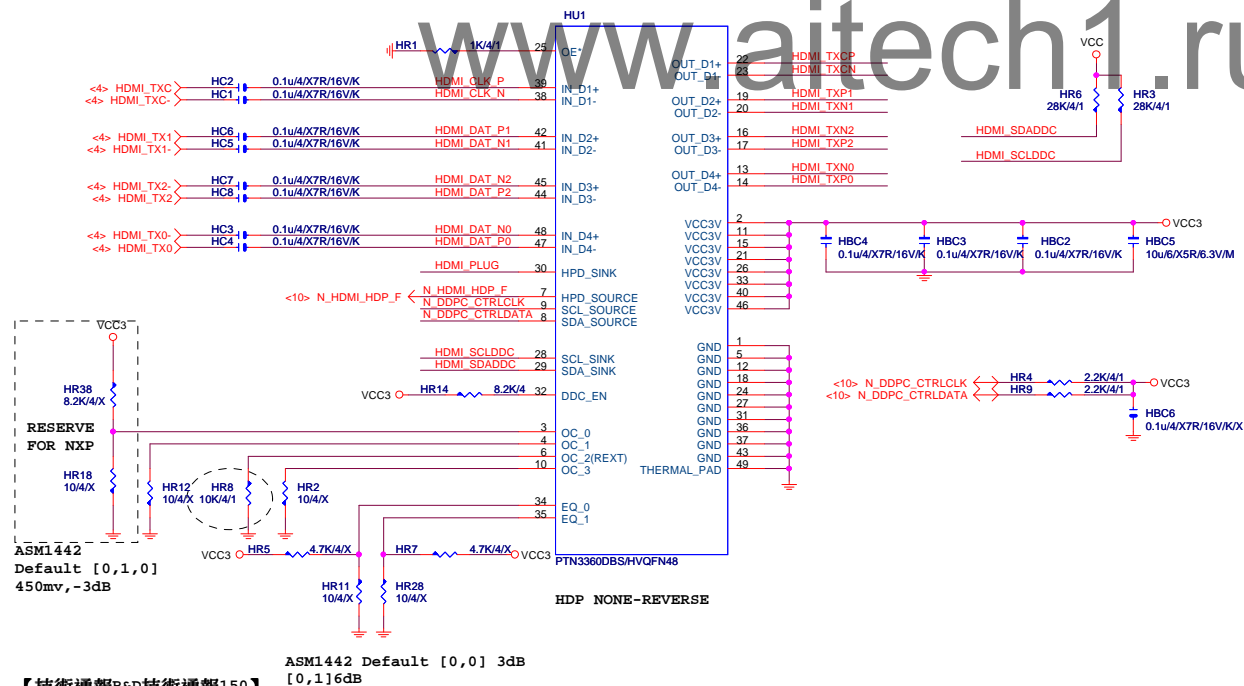
【技術通報R&D技術通報151】
33ohm Change to 68ohm



DVI LEVEL SHIFT



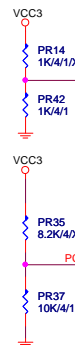
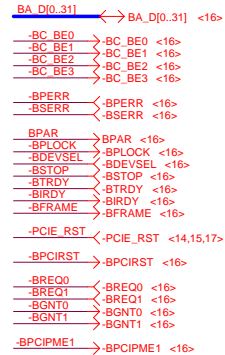
HDMI LEVEL SHIFT



【技術通報R&D技術通報150】 [0,116dB
HDMI eye diagram1.4版(deep color)會fail
原因: 目前的HDMI訊號過長,造成RISING TIME過慢,而會壓到eye diagram
改善: ASMDIA ASM1442 : 3.16K(PIN6 PULL DOWN電阻) 10ohm(PIN4 PULL DOWN電阻)

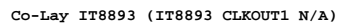
PCIE TO PCI

PCI:5/4/5 Impedance=50 +- 15%



```
High: Enable PCI CLK 66MHz
Low: Disable PCI CLK 66MHz
```

High: PCICLK INPUT form CLK Gen
Low: PCICLK OUTPUT form IT8893 chip



```
IT8892: PR24 -> 47ohm
IT8893: PR24 -> 22ohm
```

